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DPHPC: Amdahl's Law, Roofline model

Recitation session

Why do we have to do performance modelling?

- **Will my program scale?**
  "Am I going to run faster on twice larger machine?"
- **Which parts of the program I should improve?**

"Let me parallelize one more loop, that should help… I can't be spending 90% of time on communication and synchronization!"

- **Can my program achieve better performance? How far is it from maximum?**
  "I spent 50 hours on optimizing every memory accesses and I'm 0.5% faster"
- **How should we design a new computing system?**
  "Do I need accelerators? Do I need more memory?"

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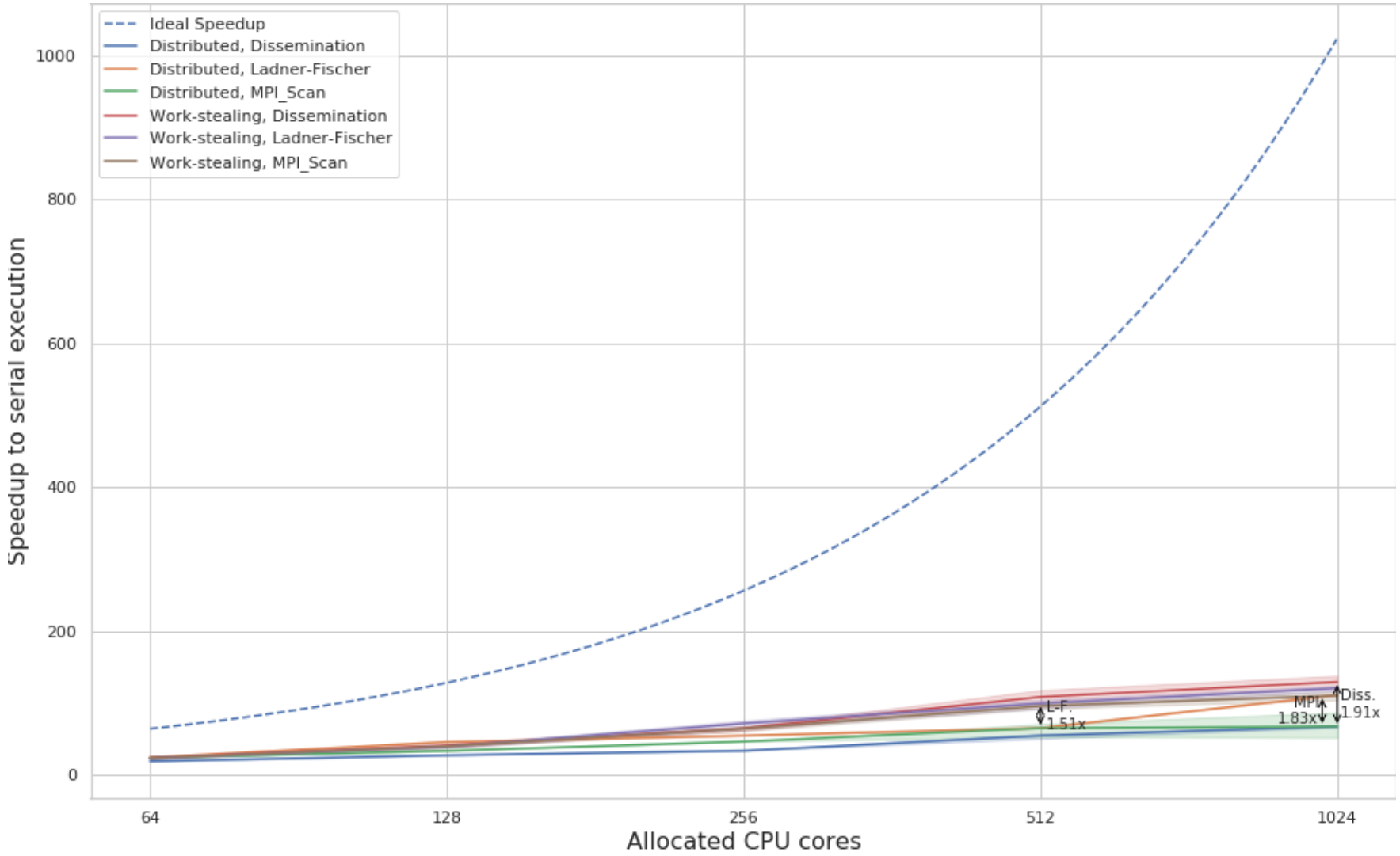
Two things we need to understand

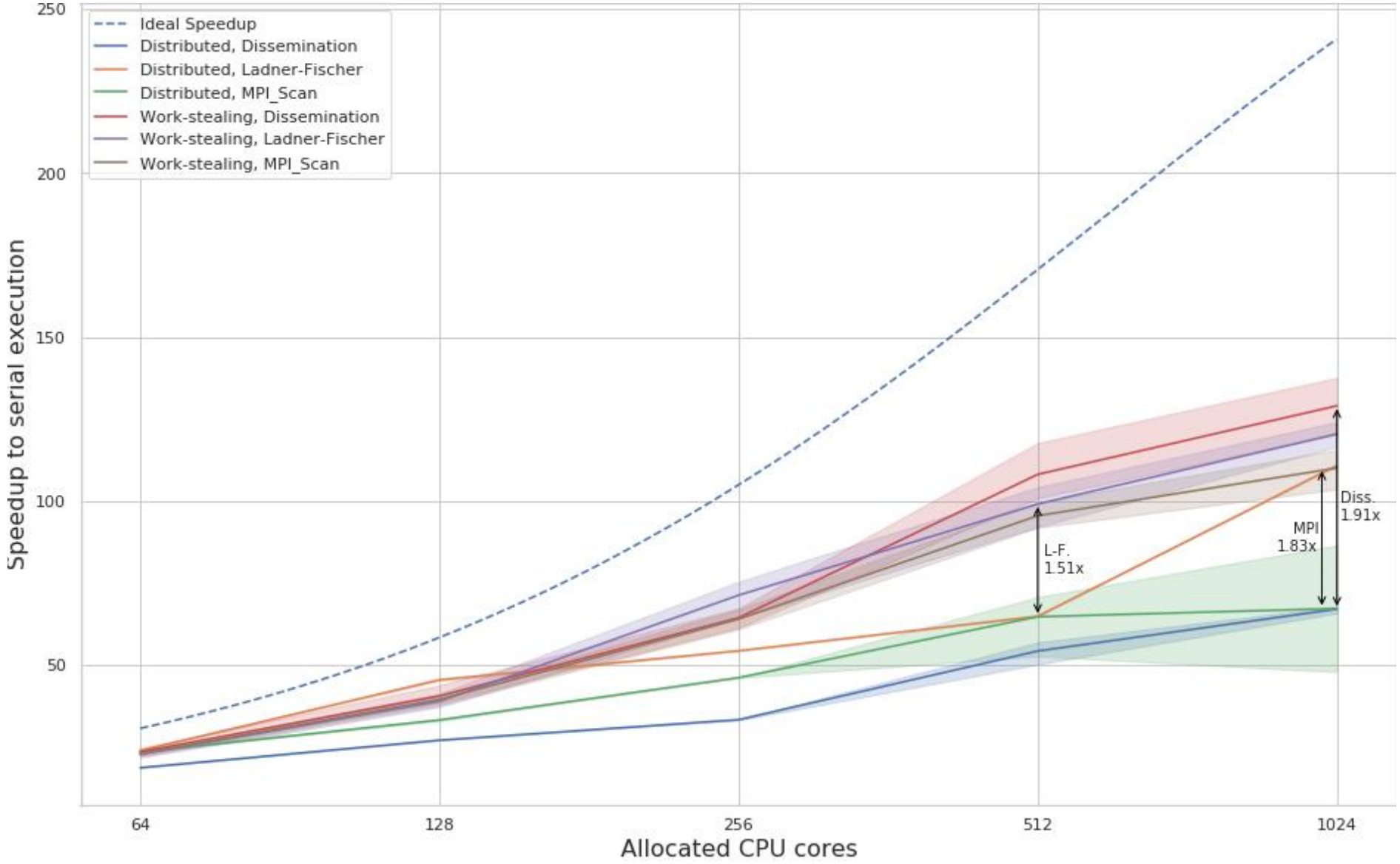
- **Baseline – slow and bad programs tend to scale better.**
- **Upper bound**

Why is upper bound important?



This is pretty pathetic…

Why is upper bound important?



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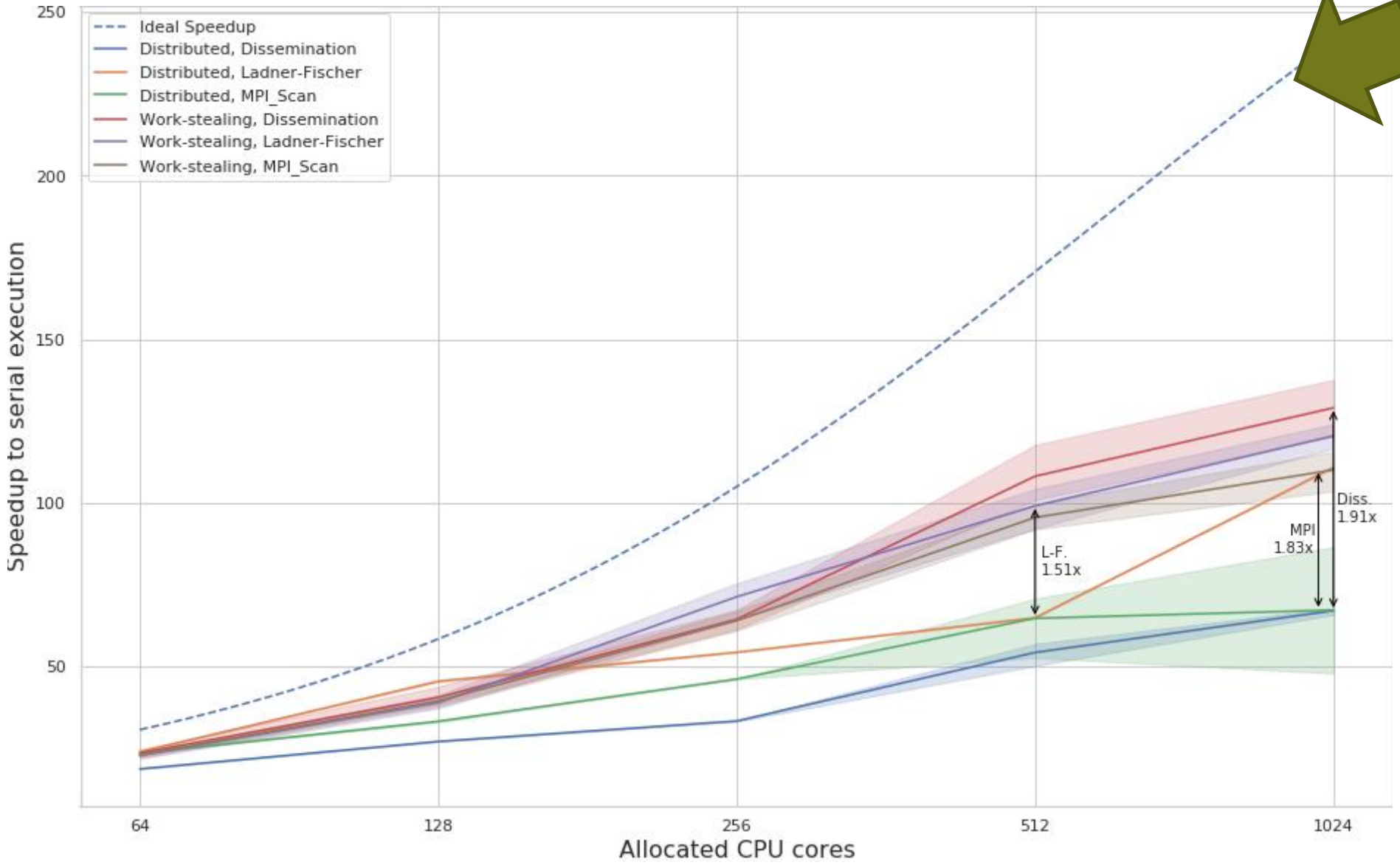

Upper bound for prefix scan

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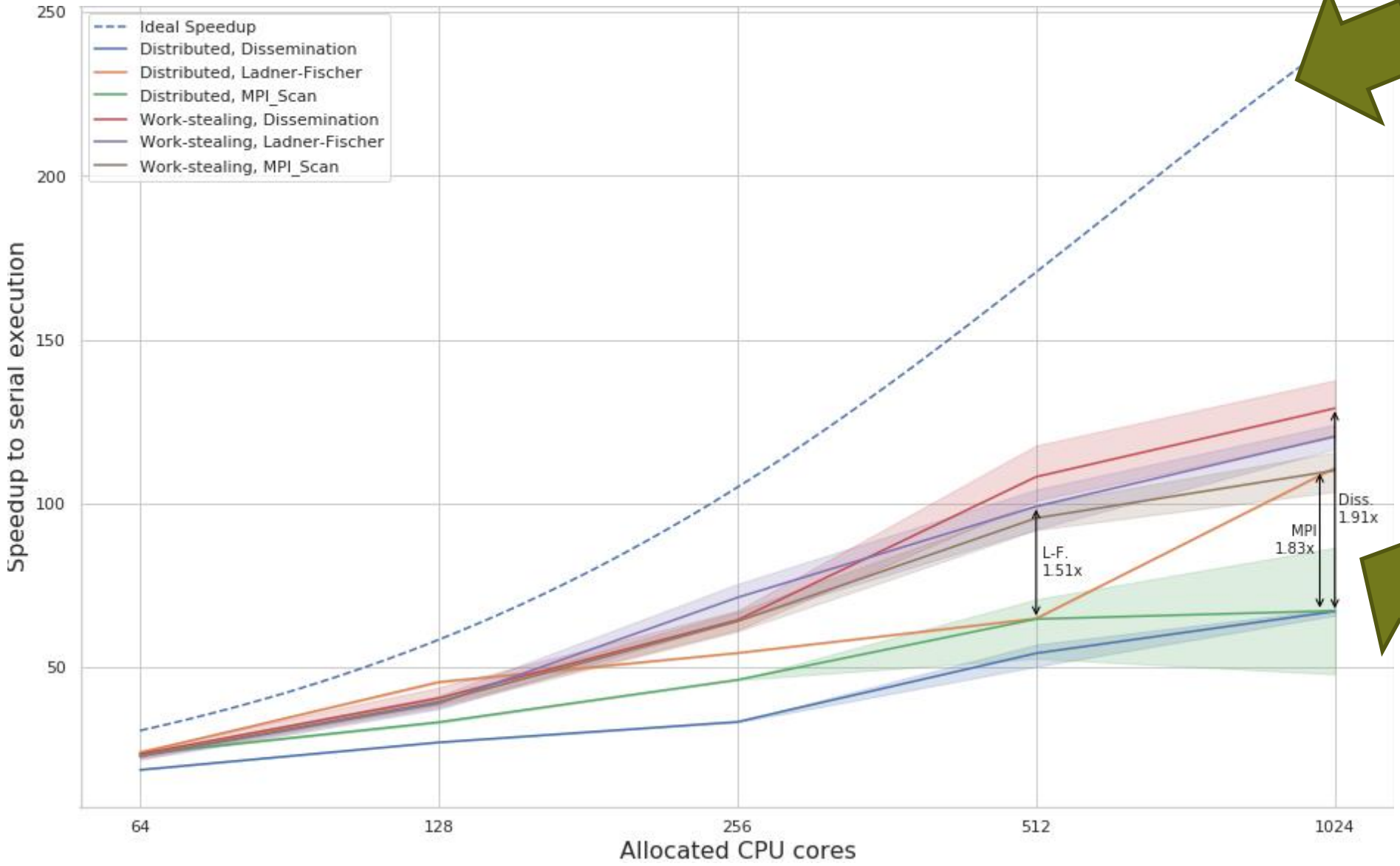

Upper bound for prefix scan

We're actually improving!

Amdahl's Law

Time of sequential program with f as the fraction not affected by the parallelization:

$$T_1 = fT_1 + (1 - f)T_1$$

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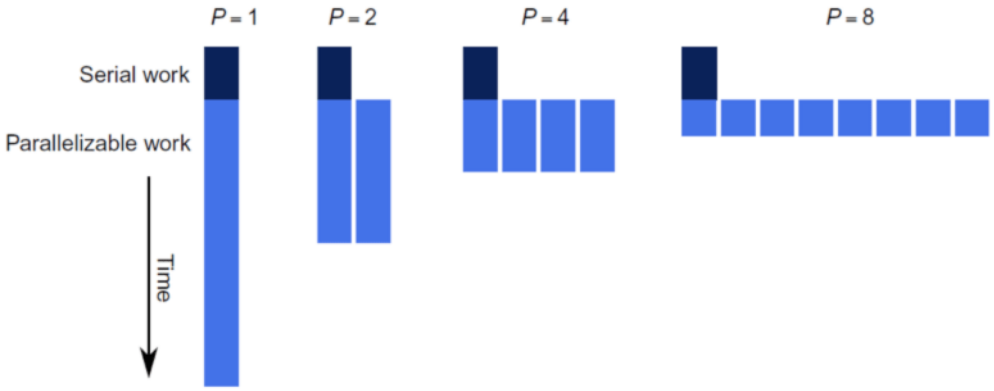

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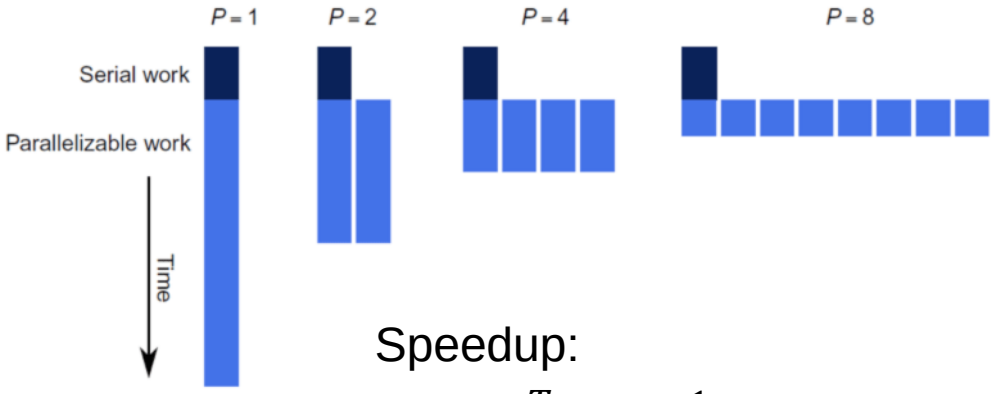

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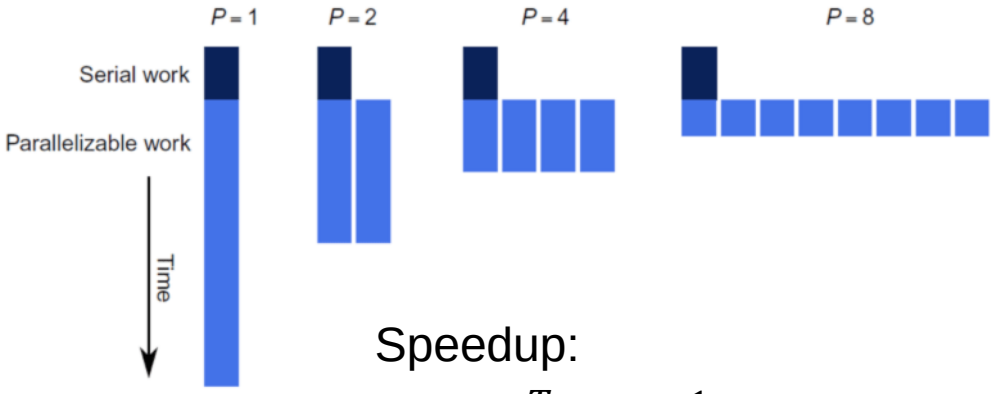

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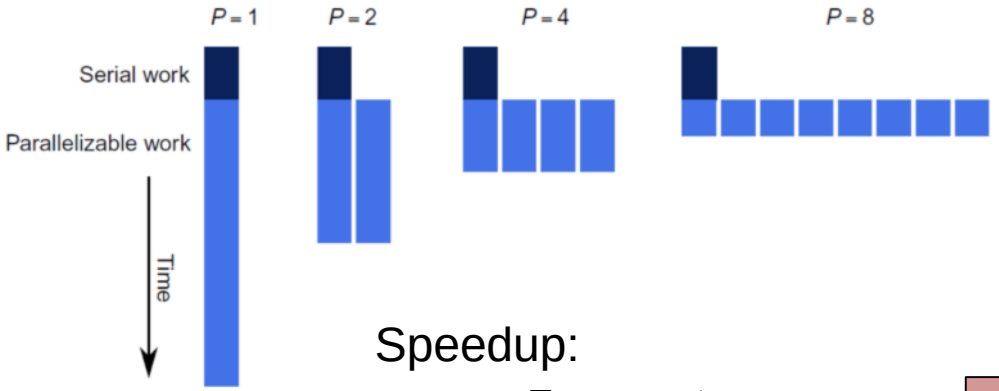

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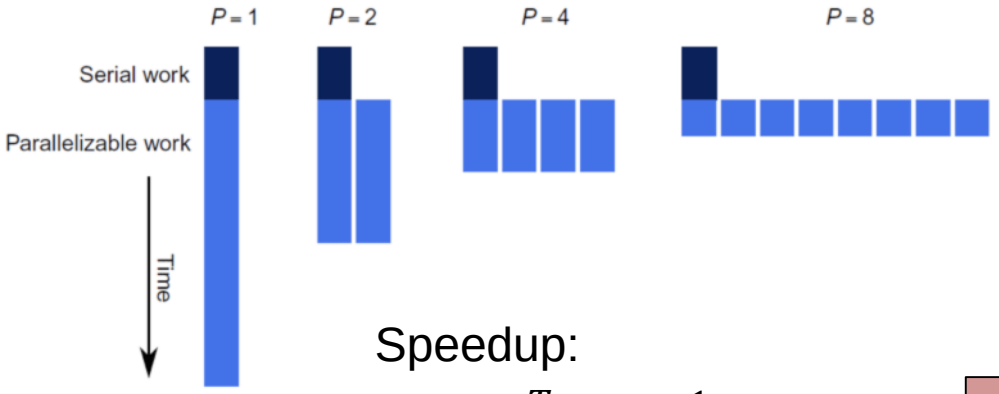

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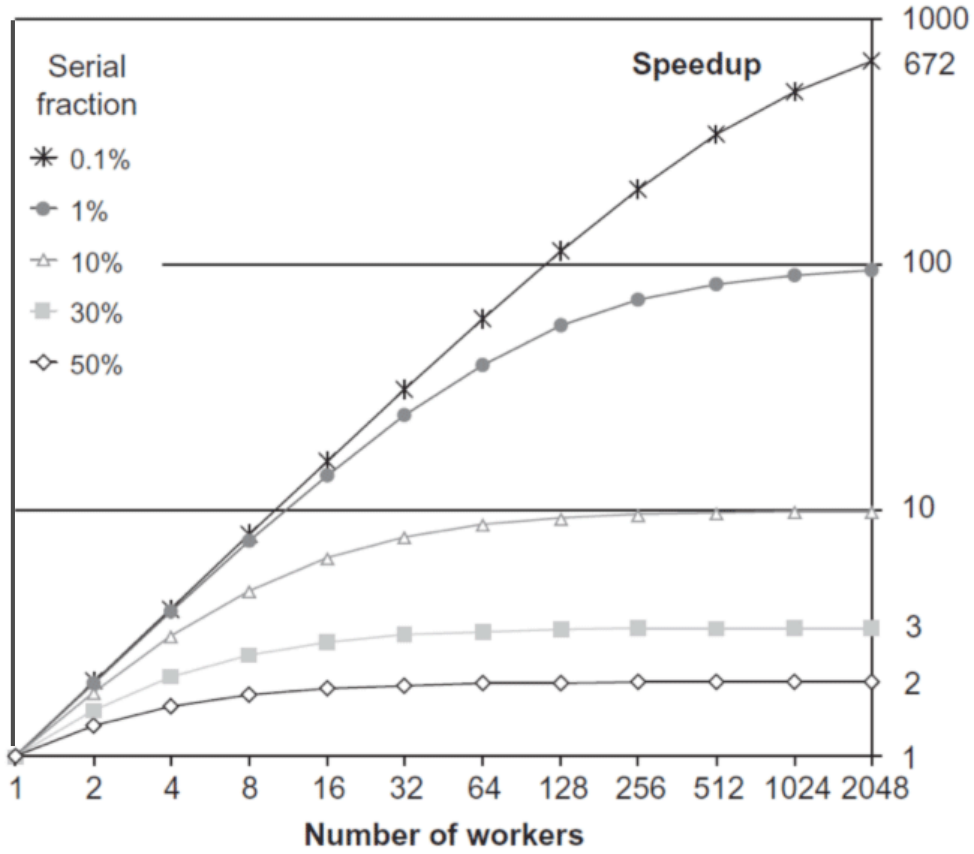


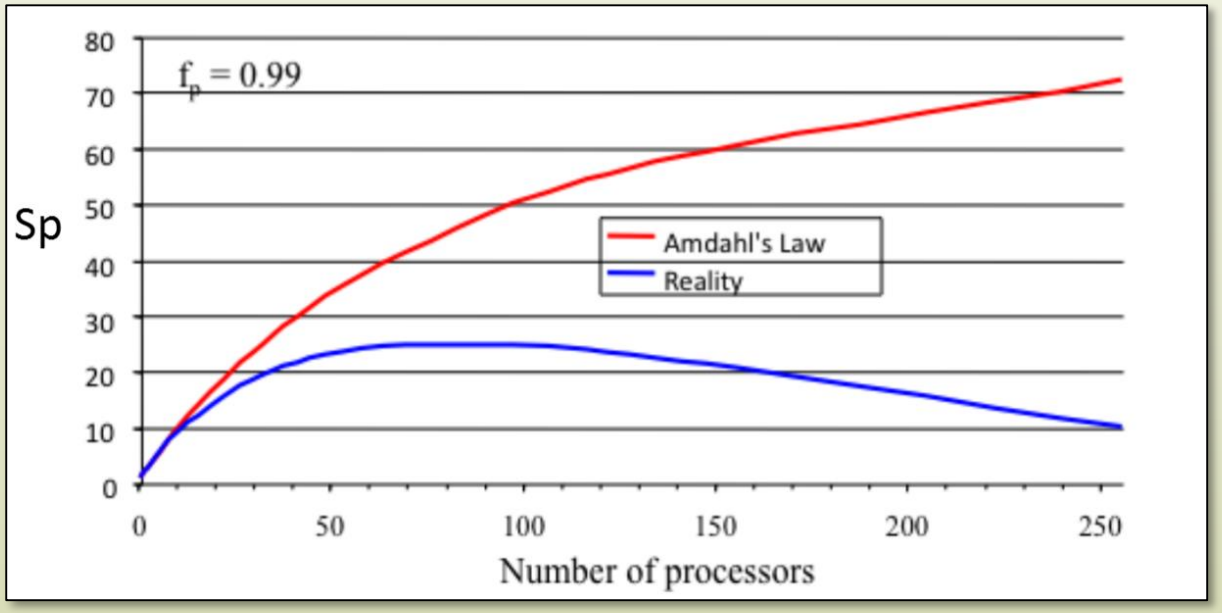
Amdahl's Law

Time of sequenti
by the parallel

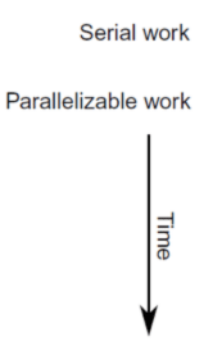
Time of paralle

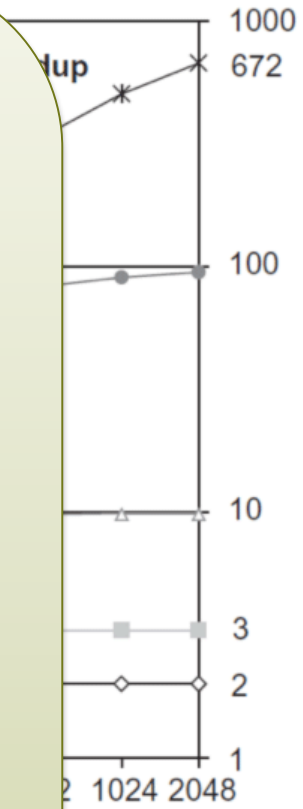
It's like to see the glass as half empty but…

It could be even worse!



Possible factors: *load balancing, communication costs, I/O, scheduling*





Amdahl’s Law vs Gustafson-Barsis' Law

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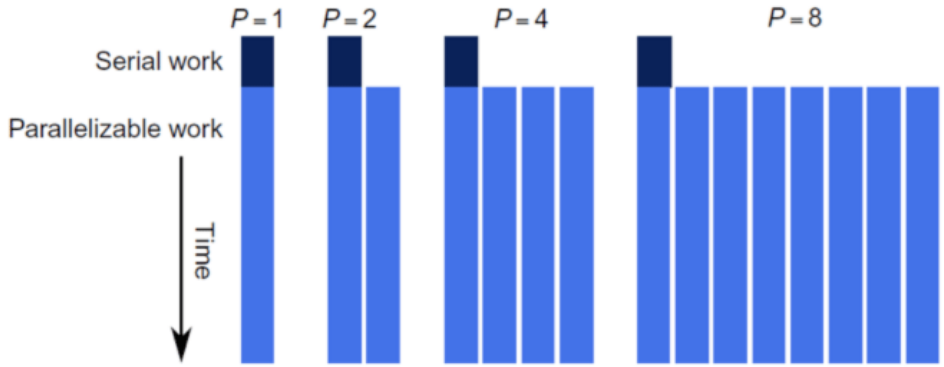

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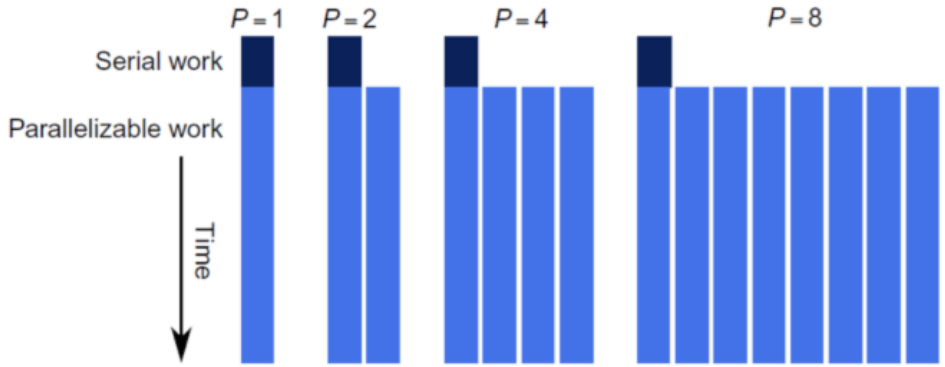

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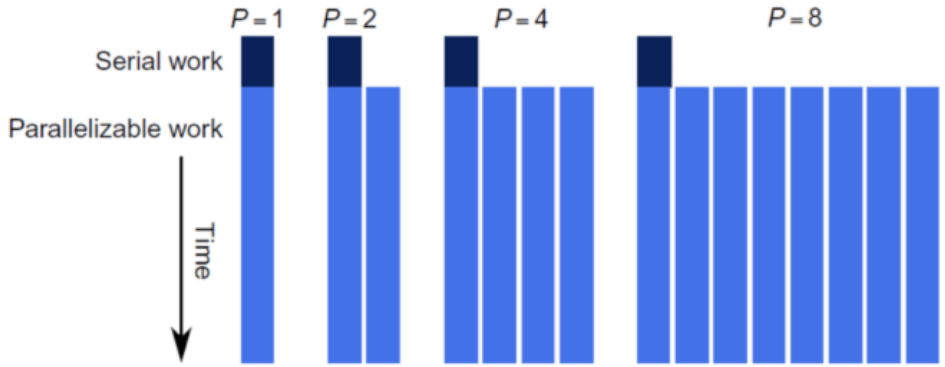

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Note: no parallel overheads are taken into account here!

Quiz

- **Speedup**
- **Efficiency**
- **Strong Scaling**
- **Weak Scaling**

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- **Speedup**
  - How well something responds to adding more resources
  - **What's your base case?** The best serial version or a single parallel process?
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Exercise 1

Assume 1% of the runtime of a program is not parallelizable. This program is run on 61 cores of a Intel Xeon Phi. Under the assumption that the program runs at the same speed on all of those cores, and there are no additional overheads, what is the parallel speedup?

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Amdahl's law assumes that a program consists of a serial part and a parallelizable part. The fraction of the program which is serial can be denoted as B — so the parallel fraction becomes $1 - B$. If there is no additional overhead due to parallelization, the speedup can therefore be expressed as

$$S(n) = \frac{1}{B + \frac{1}{n}(1 - B)}$$

For the given value of $B = 0.01$ we get $S(61) = 38.125$.

Exercise 2

Assume 0.1% of the runtime is not parallelizable. The program also invokes a broadcast operation, that add overhead depending on the number of cores involved. There are two broadcast implementations available. One adds a parallel overhead of $0.0001n$, the other one $0.0005 \log n$. For which number of cores do you get the highest speedup for both implementations?

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$$S_1(n) = \frac{1}{0.001 + \frac{1}{n}0.999 + 0.0001n}$$

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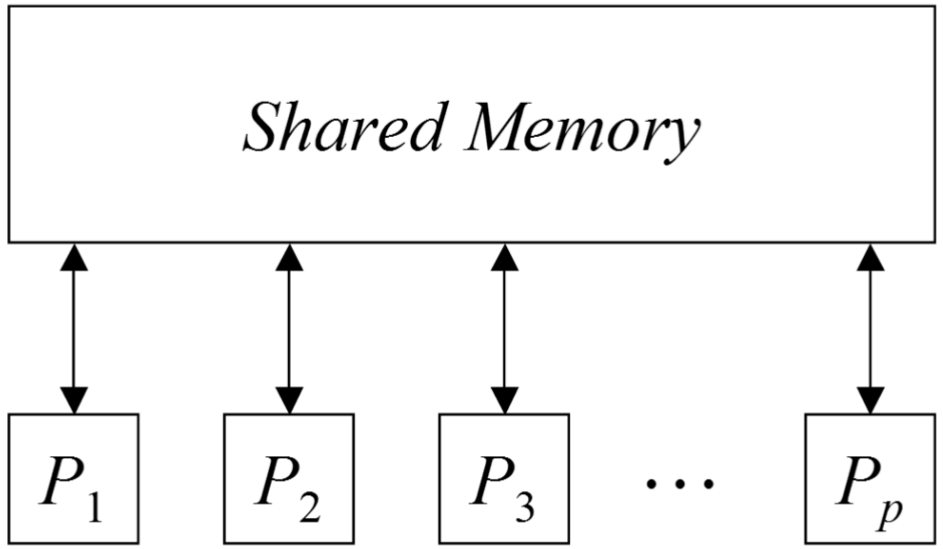
We can get the maximum of these terms if we minimize the term in denominator.

$$\frac{d}{dn}0.001 + \frac{1}{n}0.999 + 0.0001n = 0 \leftrightarrow 0.0001 - \frac{0.999}{n^2} = 0 \leftrightarrow n \approx 100$$

$$\frac{d}{dn}0.001 + \frac{1}{n}0.999 + 0.0005log(n) = 0 \leftrightarrow \frac{0.005n0.999}{n^2} = 0 \leftrightarrow n = 1998$$

PRAM: Parallel Random Access Machine

- **P processes with shared memory**
- **Ignores communications and synchronization**
- **Instruction are composed by 3 phases:**
  - Load data from shared memory (if needed)
  - Perform computation (if any)
  - Store data in shared memory (if needed)
- **Any process can read/write to any memory cell**
  - How conflicts are handled?



PRAM: Conflicting Accesses

- **EREW: Exclusive Read / Exclusive Write**
  - No two processes are allowed to read or write to the same memory cell simultaneously
- **CREW: Concurrent Read / Exclusive Write**
  - Simultaneous reads are allowed; only one process can write
- **CRCW: Concurrent Read / Concurrent Write**
  - Simultaneous reads and write to the same memory cell are allowed
  - Priority CRCW: processors assigned fixed distinct priorities, highest priority wins
  - Random CRCW: one randomly chosen write wins
  - Common CRCW: all processors are allowed to complete write if and only if all the values to be written are equal

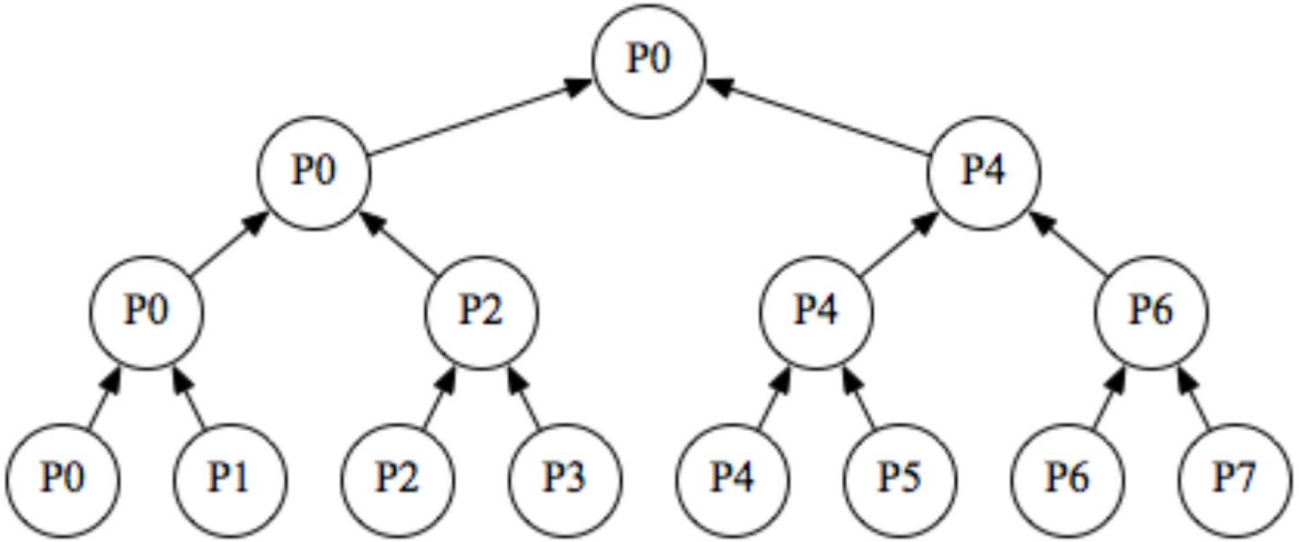
Weak **Strong**

EREW < CREW < CRCW-C < CRCW-R < CRCW-P

http://homes.cs.washington.edu/~arvind/cs424/notes/l2-6.pdf

PRAM: Reduction

- Reduce p values on the p-processor EREW PRAM in $O(logp)$ time
- The algorithm uses exclusive reads and writes
- It's the basis of other EREW algorithms

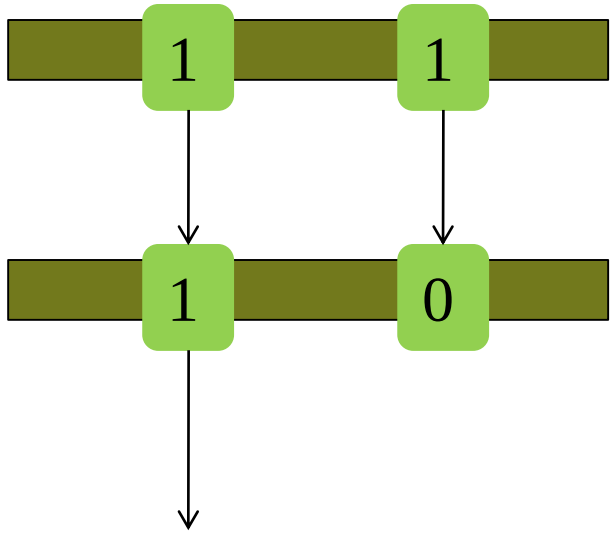


PRAM: First 1

- **Computing the position of the first one in the sequence of 0's and 1's in a constant time.**

Algorithm A
(2 parallel steps and n^2 processors)

```
for each 1≤ i<j ≤ n do in parallel
   if C[i] =1 and C[j]=1 then C[j]:=0
for each 1≤ i ≤ n do in parallel
   if C[i] =1 then FIRST-ONE-POSITION:=i
```



www.csc.liv.ac.uk/~igor/COMP308/ppt/Lect_5.ppt

PRAM: First 1 – Reducing Number of Processors

Algorithm B: it reports if there is any one in the table.

```
There-is-one:=0
for each 1≤ i ≤ n do in parallel
   if C[i] =1 then There-is-one:=1
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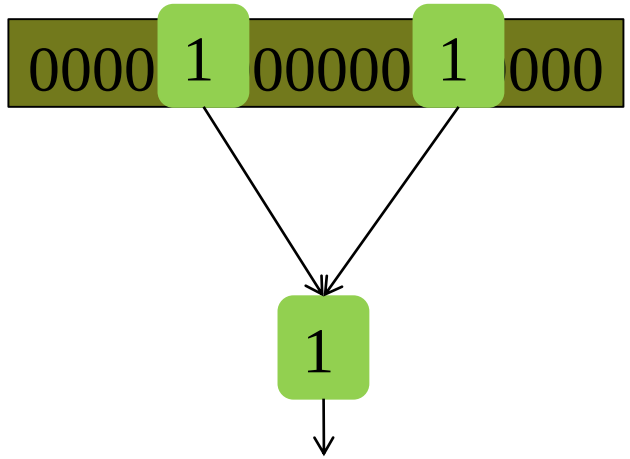

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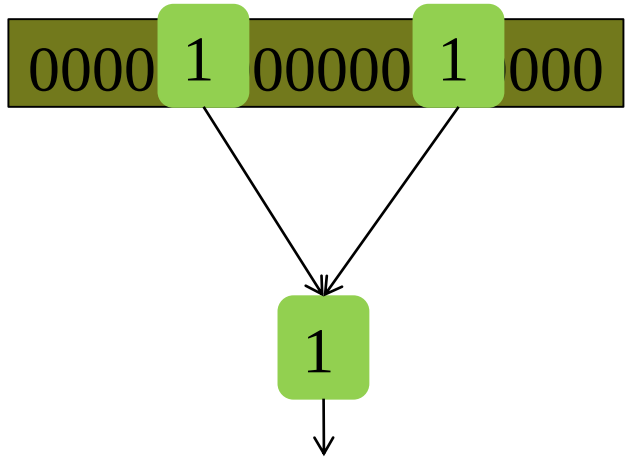
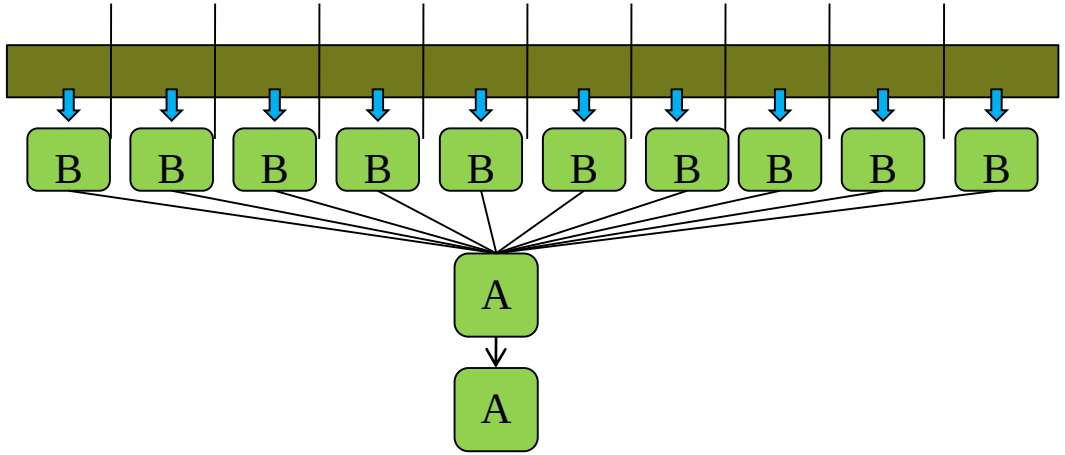


Merge A and B

1. Partition table C into segments of size $\sqrt{n}$
2. In each segment apply the algorithm B
3. Find position of the first one in these sequence by applying algorithm A
4. Apply algorithm A to this single segment and compute the final value



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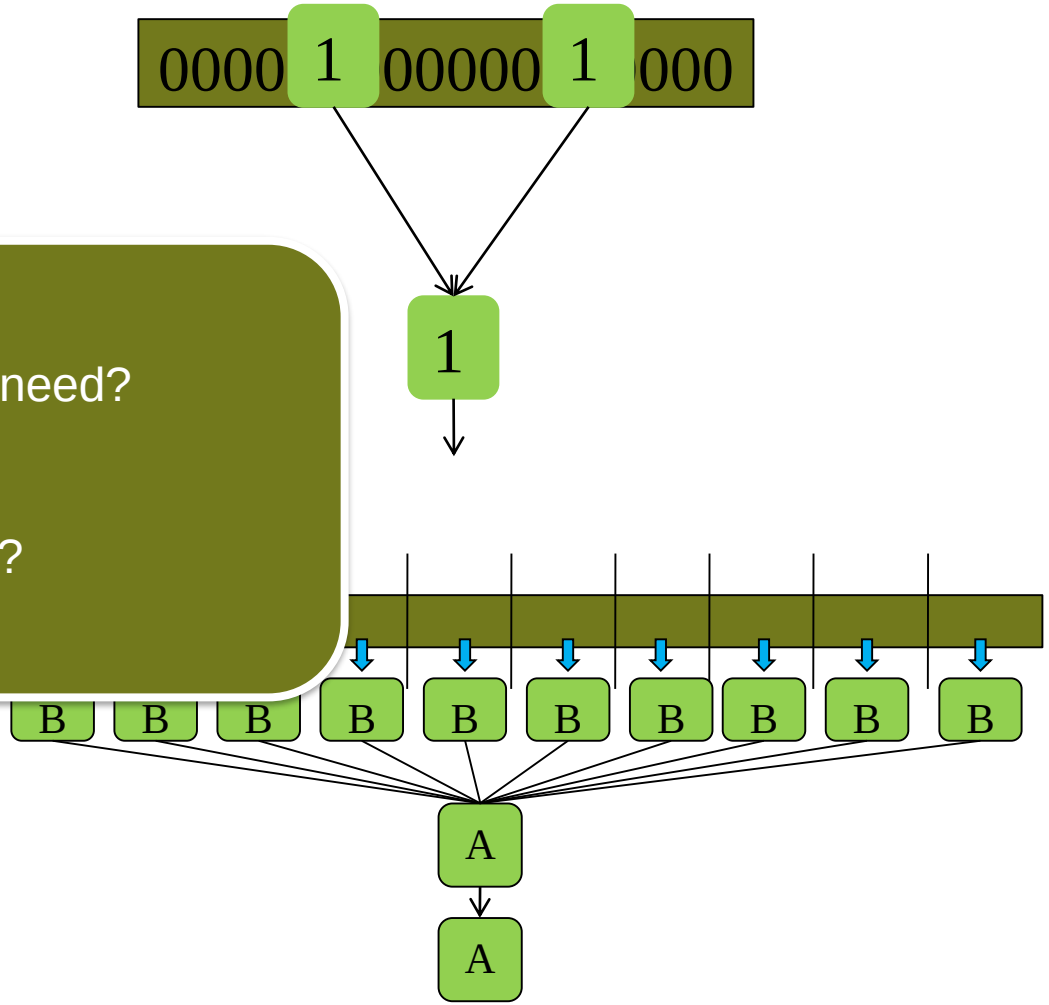
What's the complexity?



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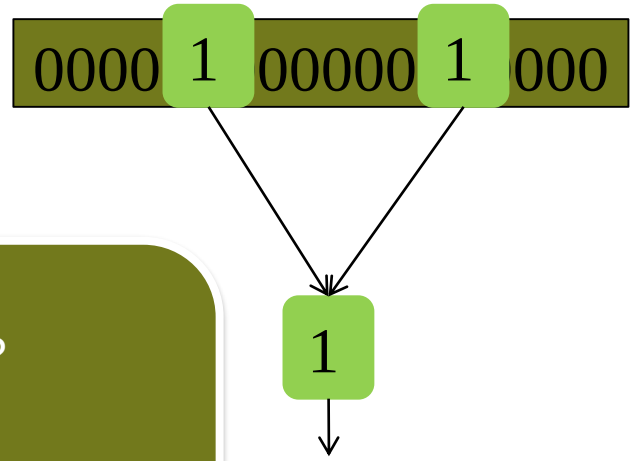
How many processors we need?
$(\sqrt{n})^2 = n$

What's the complexity?
$3\ parallel\ steps \rightarrow O(1)$



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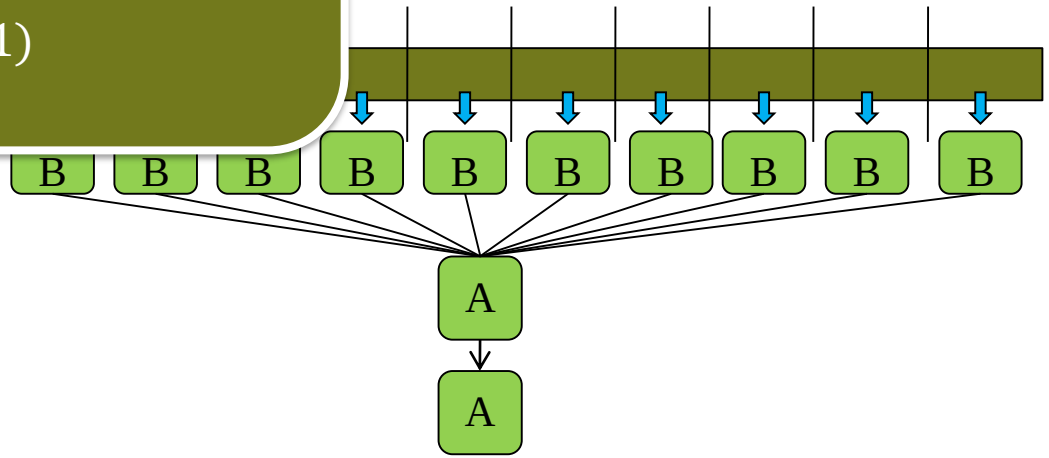

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How can we find the minimum from an unordered collection of n natural numbers on EREW-PRAM machine?

We can find the minimum from an unordered collection of n natural numbers by performing a reduction along a binary tree: In each round, each processor compares two elements, and the smaller element gets to the next round, the bigger one is discarded. What is the work and depth of this algorithm?

The dependency graph of this computation is a tree with $log_2(n)$ levels. Therefore the longest path, which is equal to the depth/span has length $log_2(n)$. The tree contains $2n - 1$ nodes, which is equal to the work.

Exercise 4

Develop an algorithm which can find the minimum in an unordered collection of n natural numbers in $O(1)$ time on a CRCW-PRAM machine.

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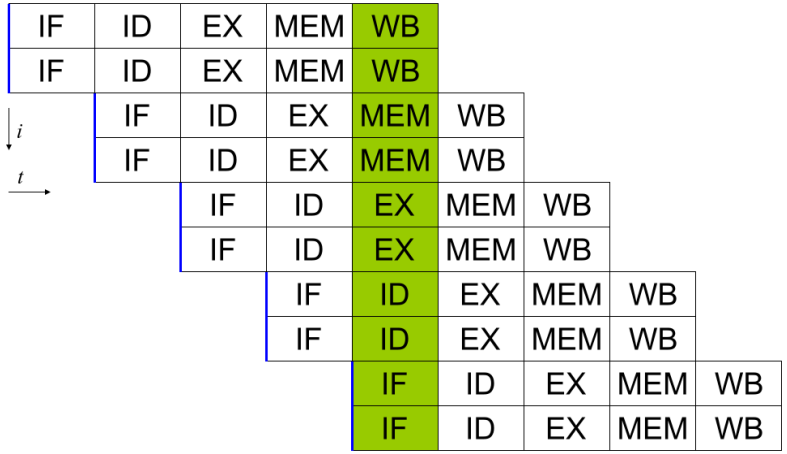
Develop an algorithm which can find the minimum in an unordered collection of n natural numbers in $O(1)$ time on a CRCW-PRAM machine.

- Assume the list is stored in an array A.
- Create an additional array $tmp[n]$ initialized with $true$.
- We use $O(n^2)$ processors, labelled $p(i,j)$ with $0 \leq i,j \leq n$.
- Each processor $p(i,j)$ checks if $A[i] > A[j]$.
  - If true then $tmp[i]$ is set to false (it cannot be the minimum)
  - Otherwise nothing is done
- At the end we have only one element of tmp set to true, say $tmp[k]$. The minimum element of A is $A[k]$.

Computation

- **Usually, floating point performance (Gflop/s) is the metric of interest**
- **Road to peak in-core performance:**



Instruction Level Parallelism (ILP)

Computation

- **Usually, floating point performance (Gflop/s) is the metric of interest**
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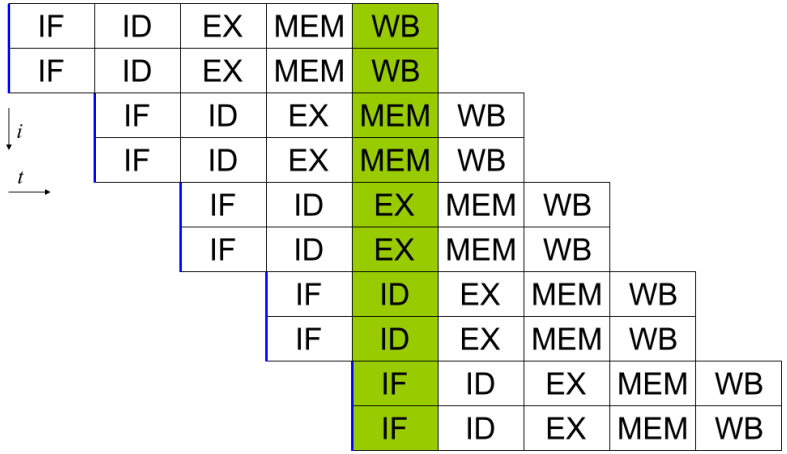
  - ***Improve ILP and apply SIMD***



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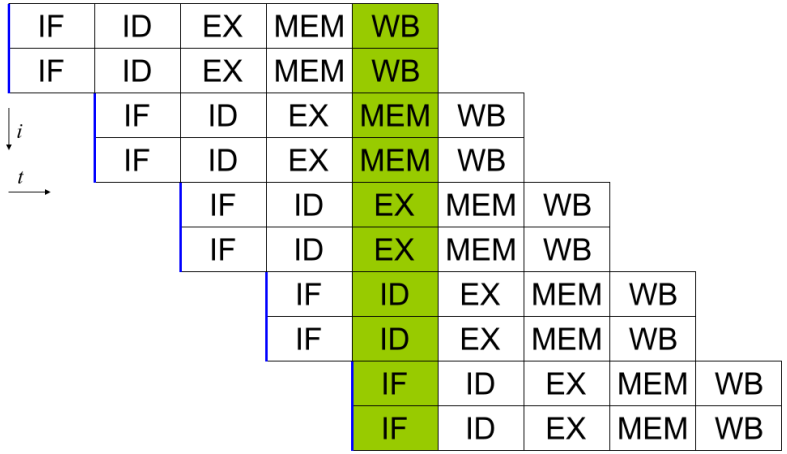

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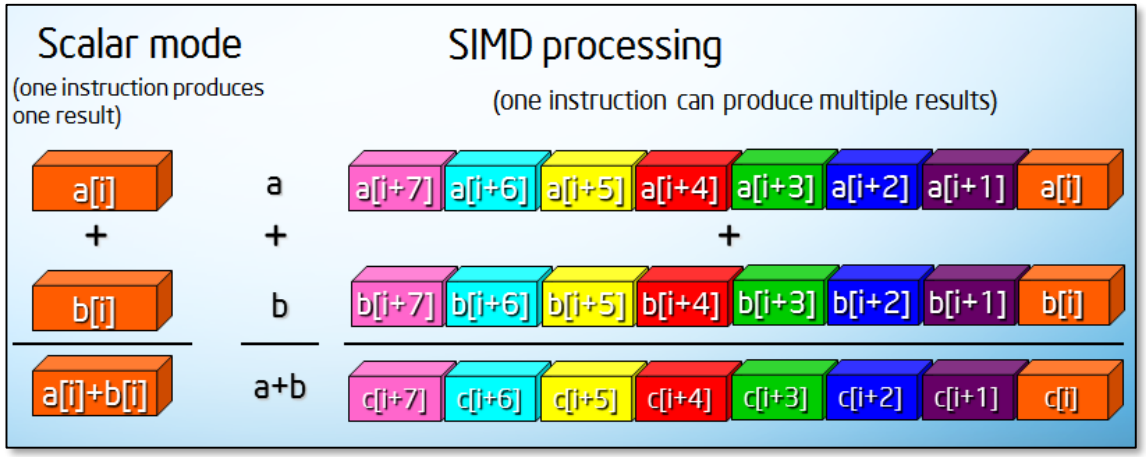

Single Instruction Multiple Data (SIMD)

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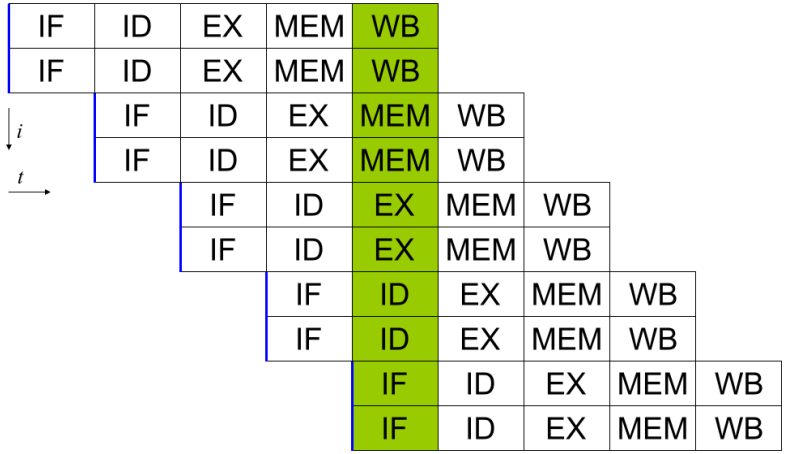

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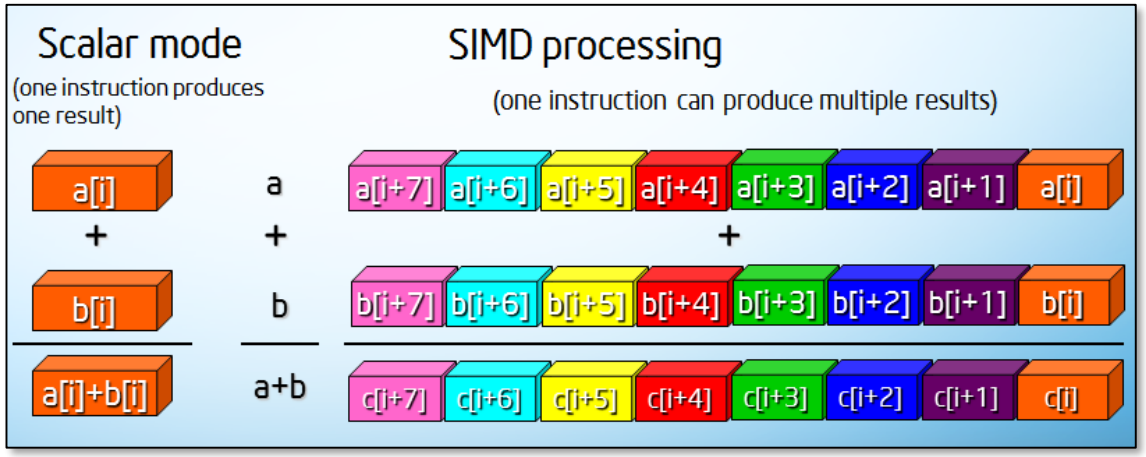

Single Instruction Multiple Data (SIMD)

- ***Balance floating-point operation mix:*** equal number of additions and multiplications

  Hardware may have Fused Multiple-Add instructions (FMA) or equal number of adders/multipliers

Communication

- **DRAM bandwidth (GB/s) is the metric of interest**

```
for (i=0; i<n; i++)
   for (j=0; j<n; j++)
      a[i][j] = a[i][j] + c[i][j] * d;
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for (i=0; i<n; i++)
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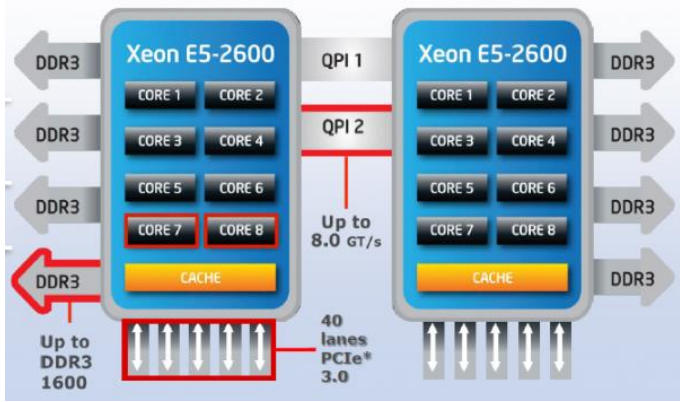

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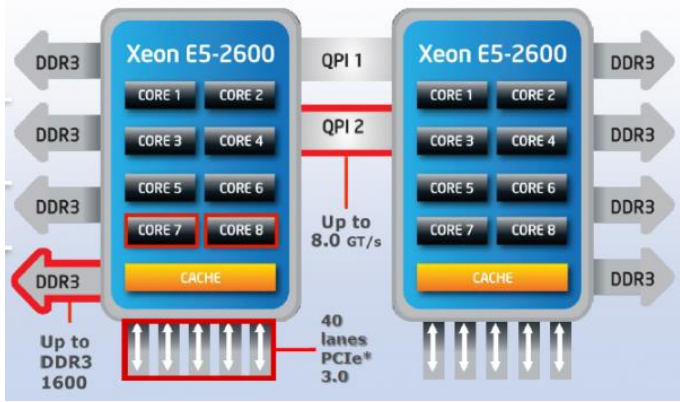

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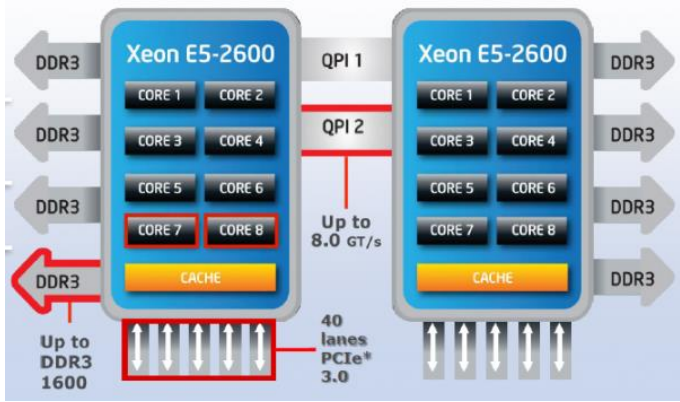

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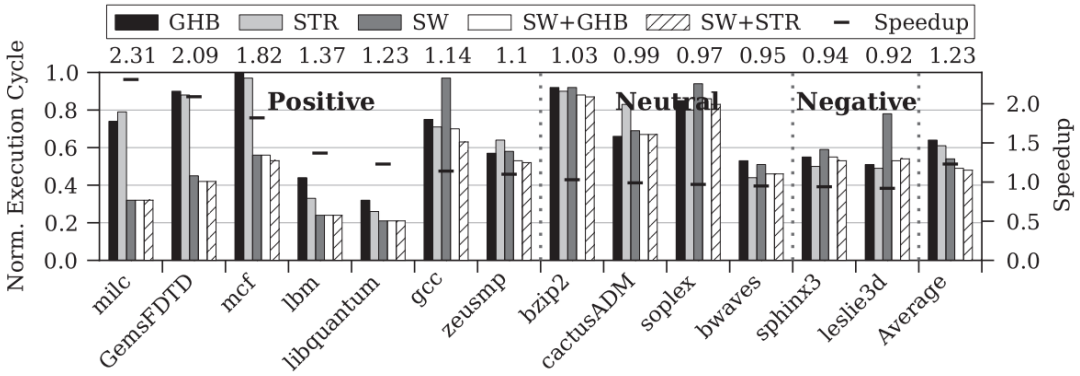

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Locality

- **3Cs Model**
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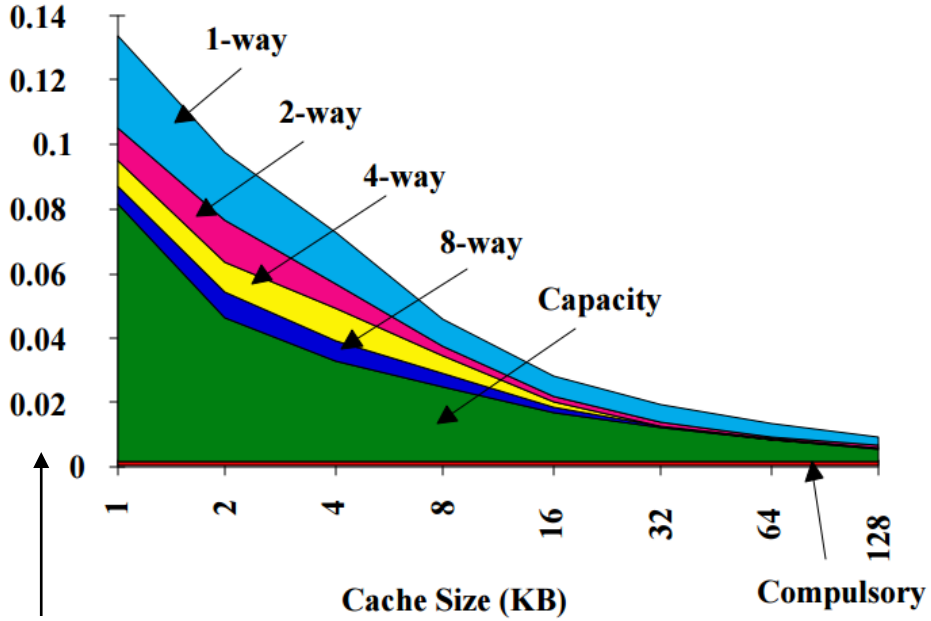

Absolut Miss Rates
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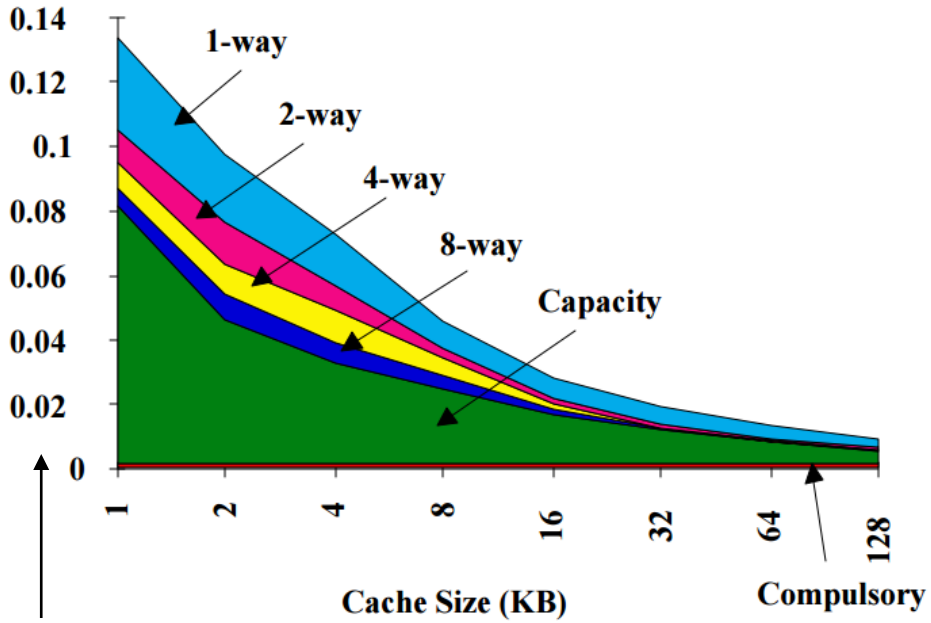

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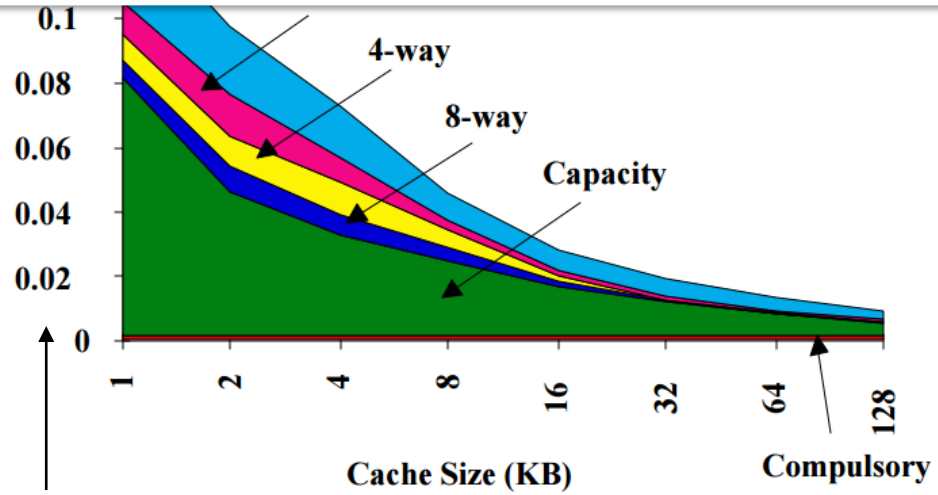

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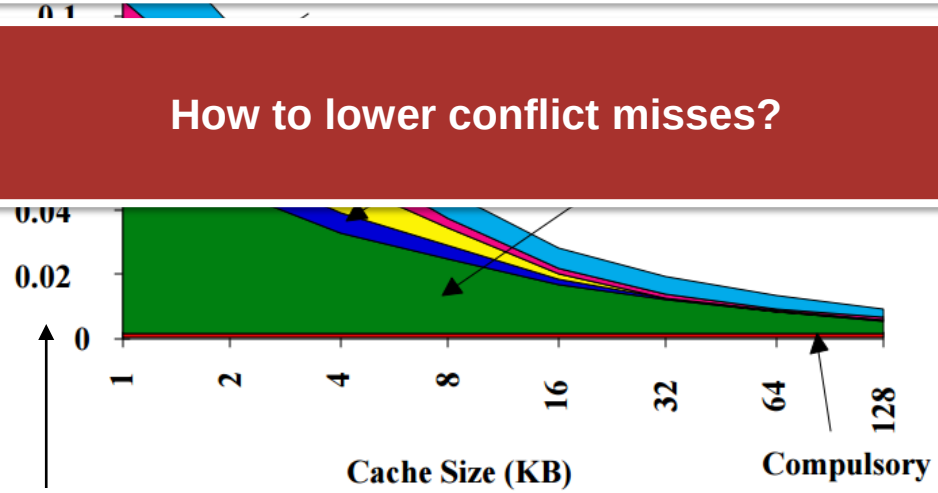

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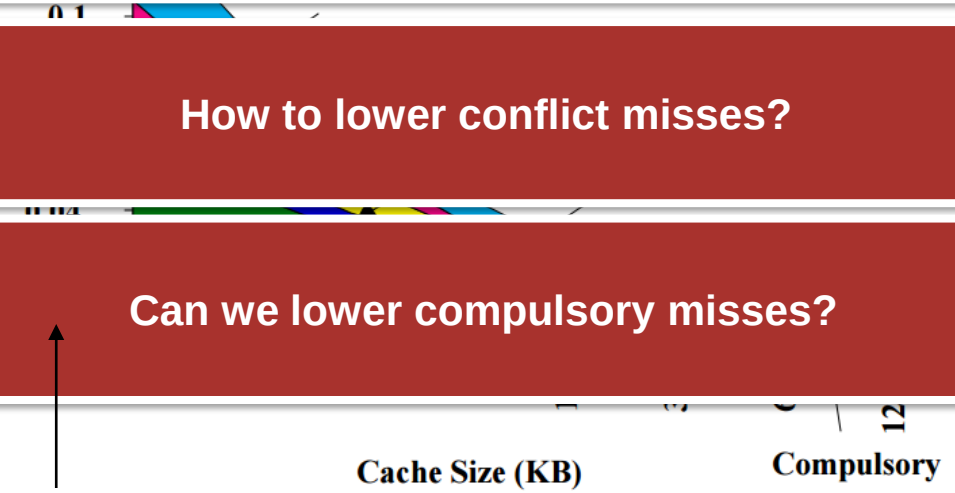

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How to Improve Locality?

- **Merging Arrays**

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/* Before: 2 sequential arrays */
int val[SIZE];
int key[SIZE];

/* After: 1 array of stuctures */
struct merge {
   int val;
   int key;
};
struct merge merged_array[SIZE];
```

- **Loop Interchange**
- **Loop Fusion**
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- Reduce conflicts between key and val
- Improve spatial locality

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How to Improve Locality?

- **Merging Arrays**
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```
/* Before */
for (k = 0; k < 100; k = k+1)
   for (j = 0; j < 100; j = j+1)
        for (i = 0; i < 5000; i = i+1)
              x[i][j] = 2 * x[i][j];
/* After */
for (k = 0; k < 100; k = k+1)
   for (i = 0; i < 5000; i = i+1)
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Improves spatial locality: sequential access instead of striding through memory every 100 words

- **Loop Fusion**
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How to Improve Locality?

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```
/* Before */
for (i = 0; i < N; i = i+1)
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- From two missies per access to a & c to one miss per access
- Improve temporal locality

- **Blocking or "tiling"**

How to Improve Locality?

- **Merging Arrays**
- **Loop Interchange**
- **Loop Fusion**
- **Blocking or “tiling”**
  - Example: matrix multiplication
  - Goal: reduce the working set

Compute/Memory Bound

- **What do we mean by “compute bound”?**
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- **They're not very precise definitions…**
- **Roofline model helps to clarify**
  - Plots the performance (GFlops/second) as a function of the Operational Intensity (GFlops/byte)
  - What's Operational Intensity?

Operational Intensity

How many Flops per byte does your code show?

- **Work:** W is the number of operations performed by a given program
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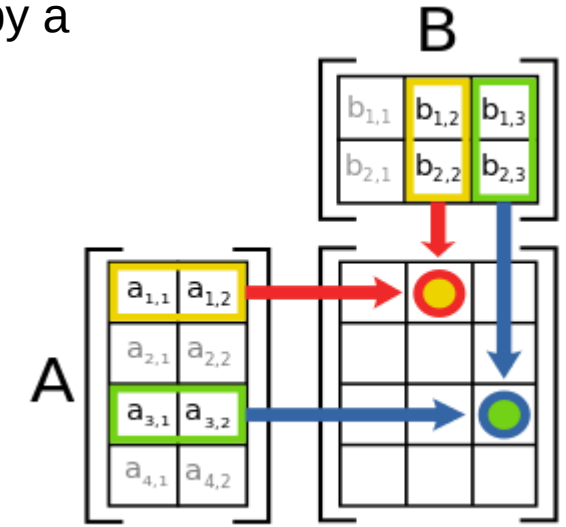

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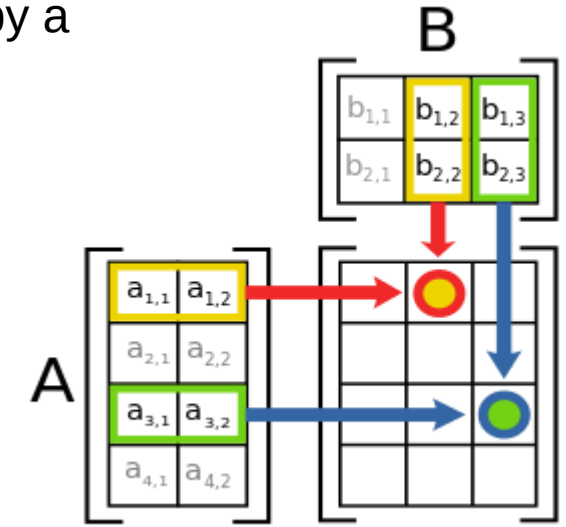

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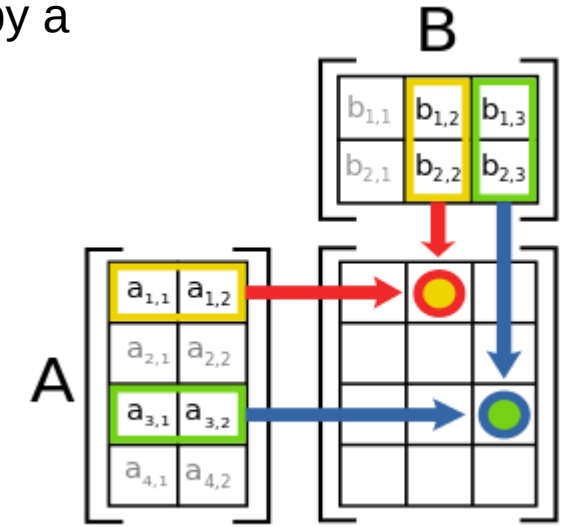

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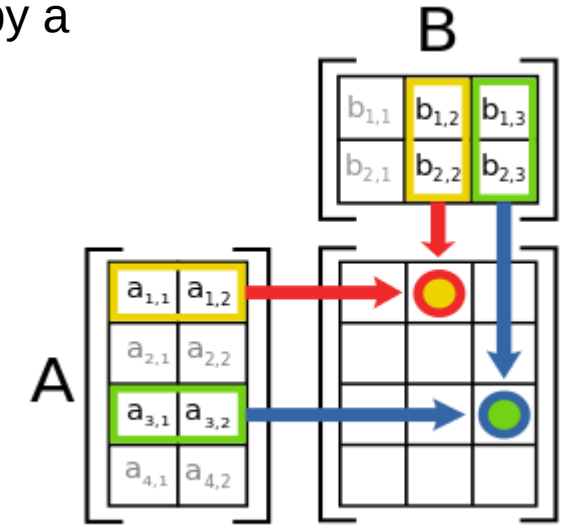

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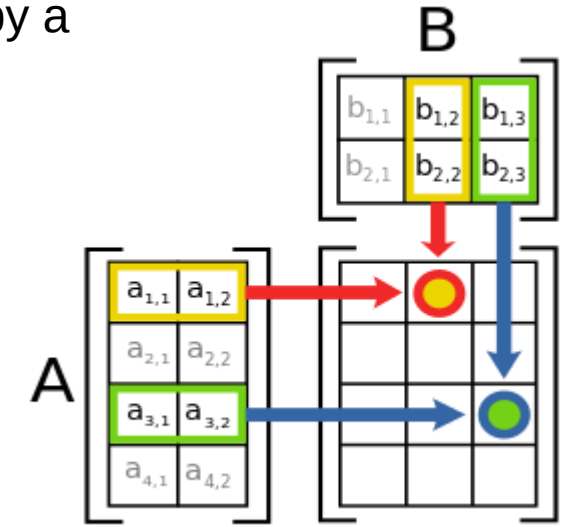

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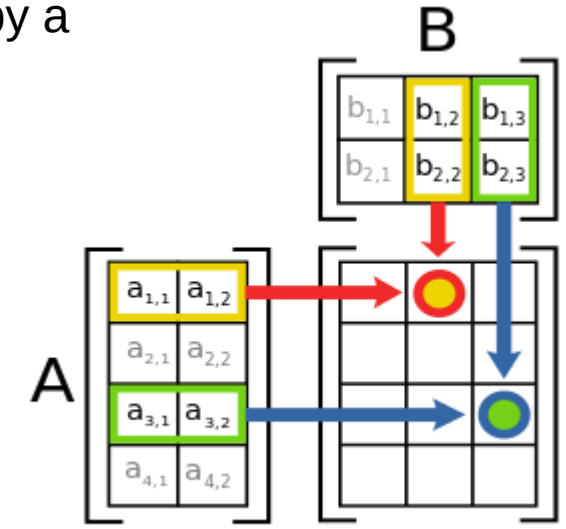
  - **Example:** matrix multiplication (3 nested loops)

$$W(n) = \sim n^3$$
$$Q(n) = n^2$$

$$I(n) = \frac{W(n)}{Q(n)} = \sim n$$



Operational Intensity

- **How many Flops per byte does your code show?**
  - **Work:** W is the number of operations performed by a given program
  - **Memory Traffic:** Q is the number of bytes transferred from memory by a given program

- **Can you increase it?**
  - For some kernels, OI is a function of the input size

    e.g., dense matrix multiplication
  - What else?

    Improve locality

  - **Example:** matrix multiplication (3 nested loops)

$$W(n) = \sim n^3$$
$$Q(n) = n^2$$

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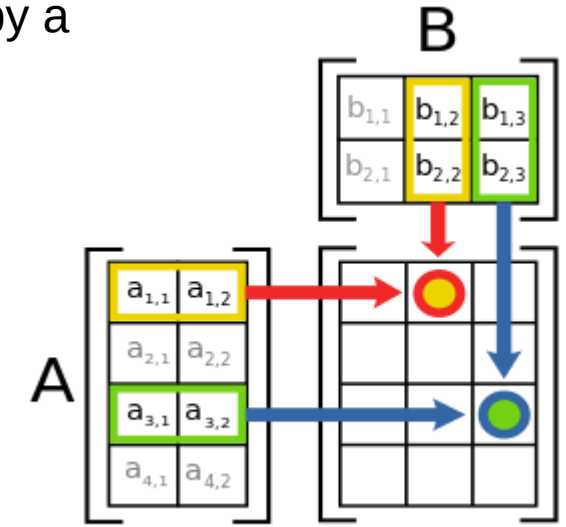


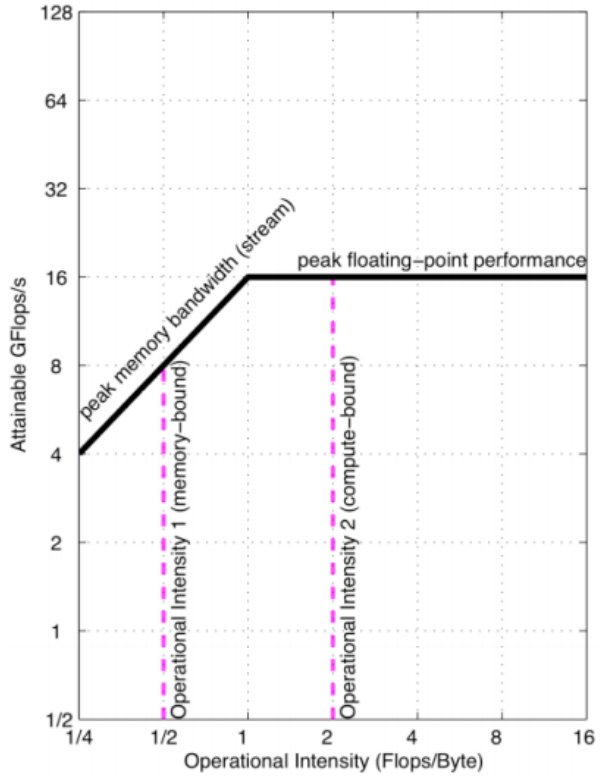
Measures the traffic between the caches and DRAM. But why?

Roofline Model

Attainable GFlops/sec = Min(Peak Floating Point Performance,
Peak Memory Bandwidth x Operational Intensity)

- **A kernel with a given OI lies somewhere in the vertical line with x=OI**

- **Ridge point:** intersection of the diagonal and horizontal roof
  - *Its x-coordinate is the minimum operational intensity required to achieve maximum performance*
  - *It suggests the level of difficulty for programmers and compiler writers to achieve peak performance*



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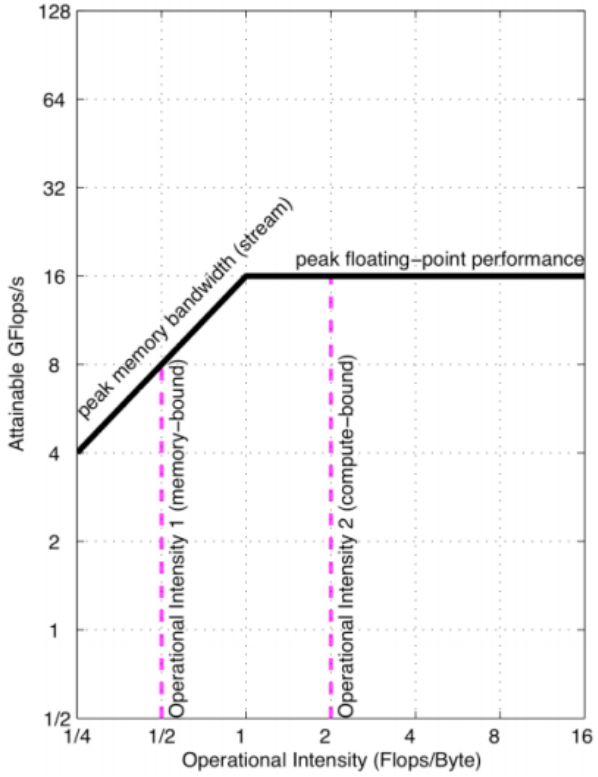

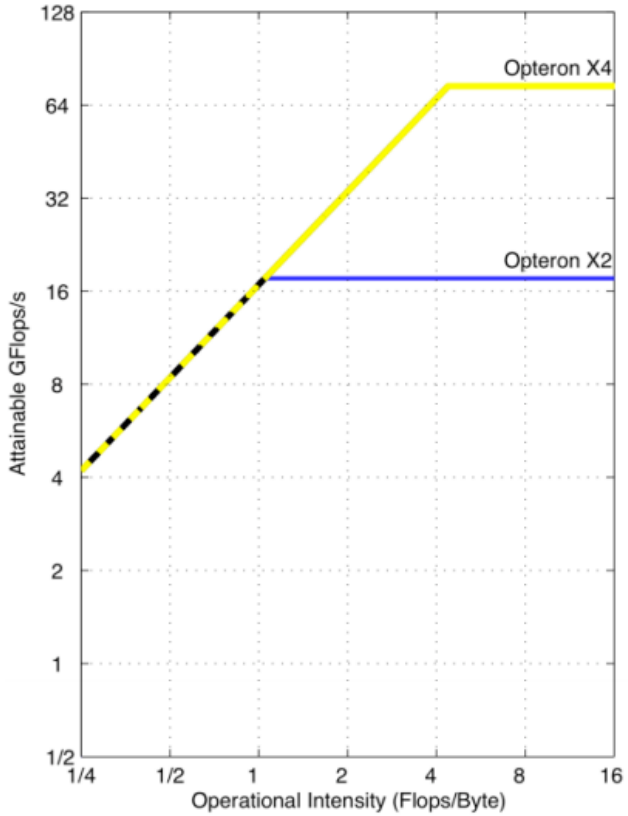

Opteron X4:

- Can issue 2 FP SSE2 instructions per cycle
- Slightly faster clock rate
- >4x gain in peak performance w.r.t. X2

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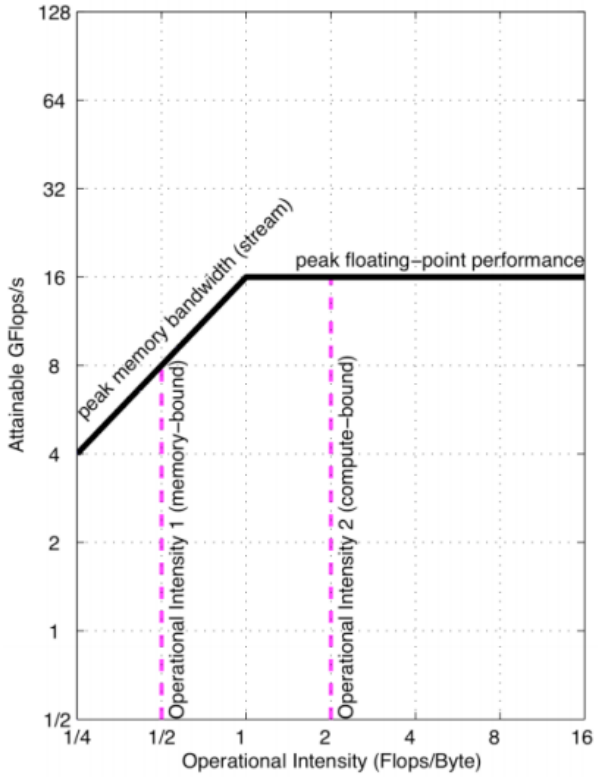

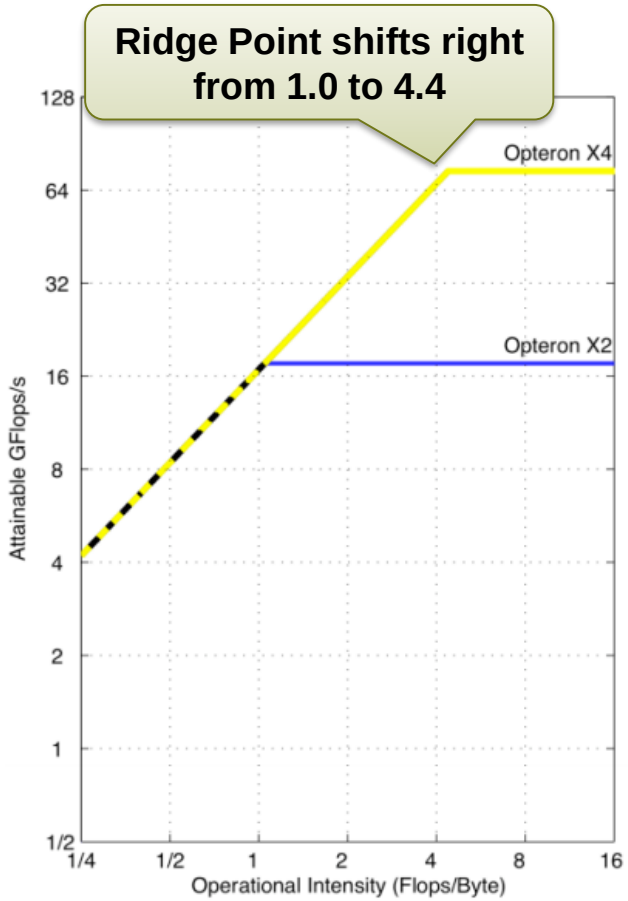

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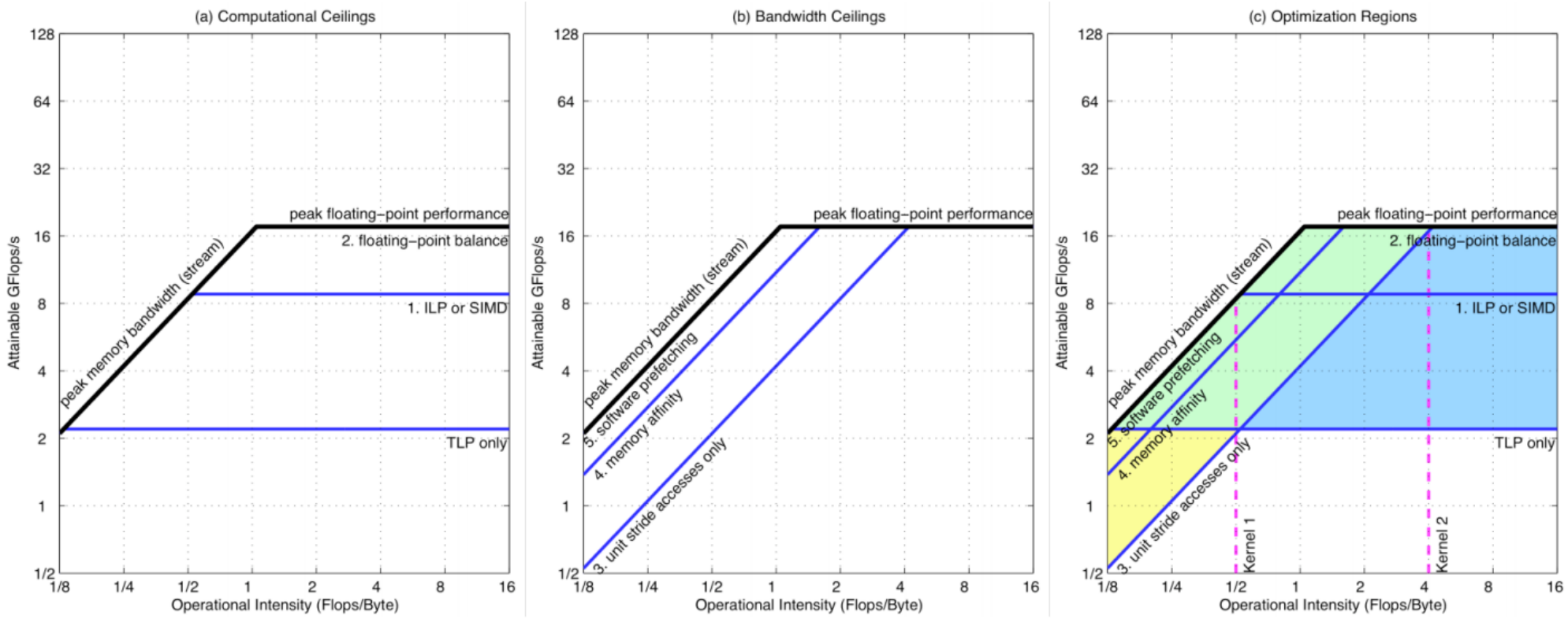
Adding Ceilings

- **What if your program is far from the roofline?**



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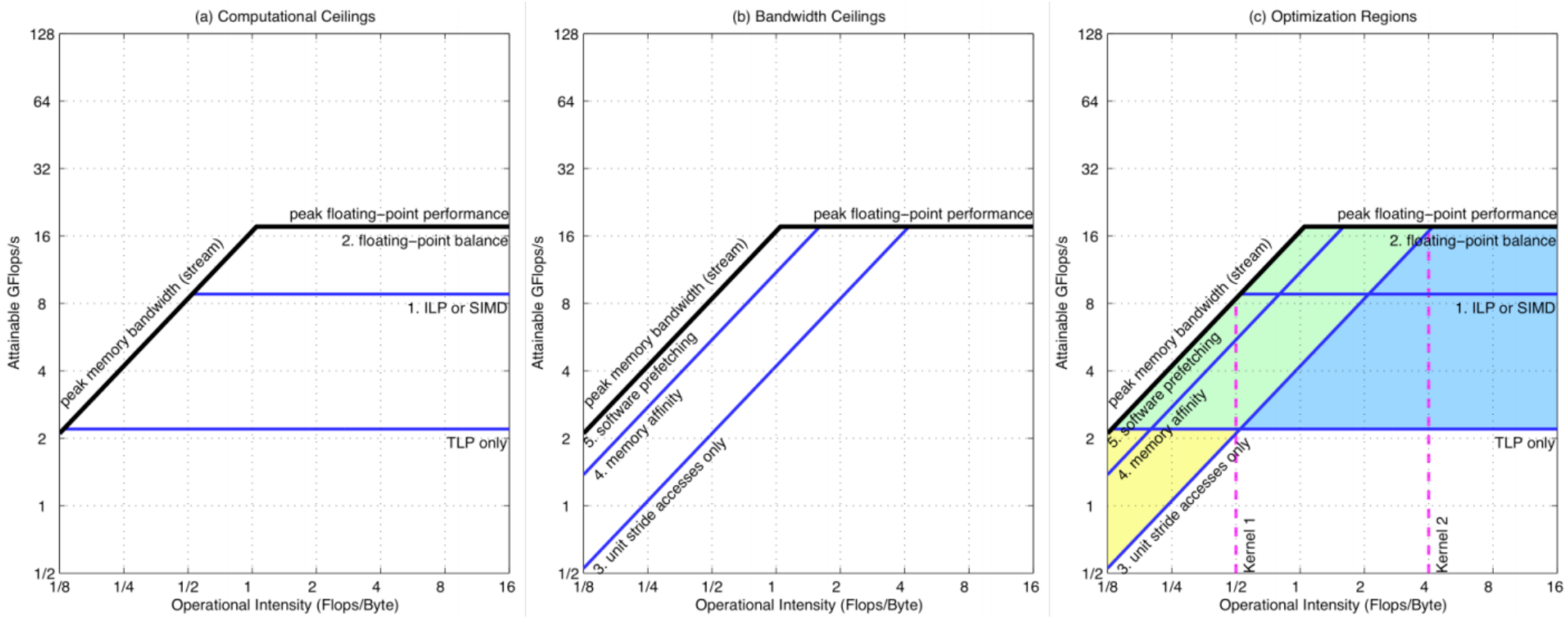

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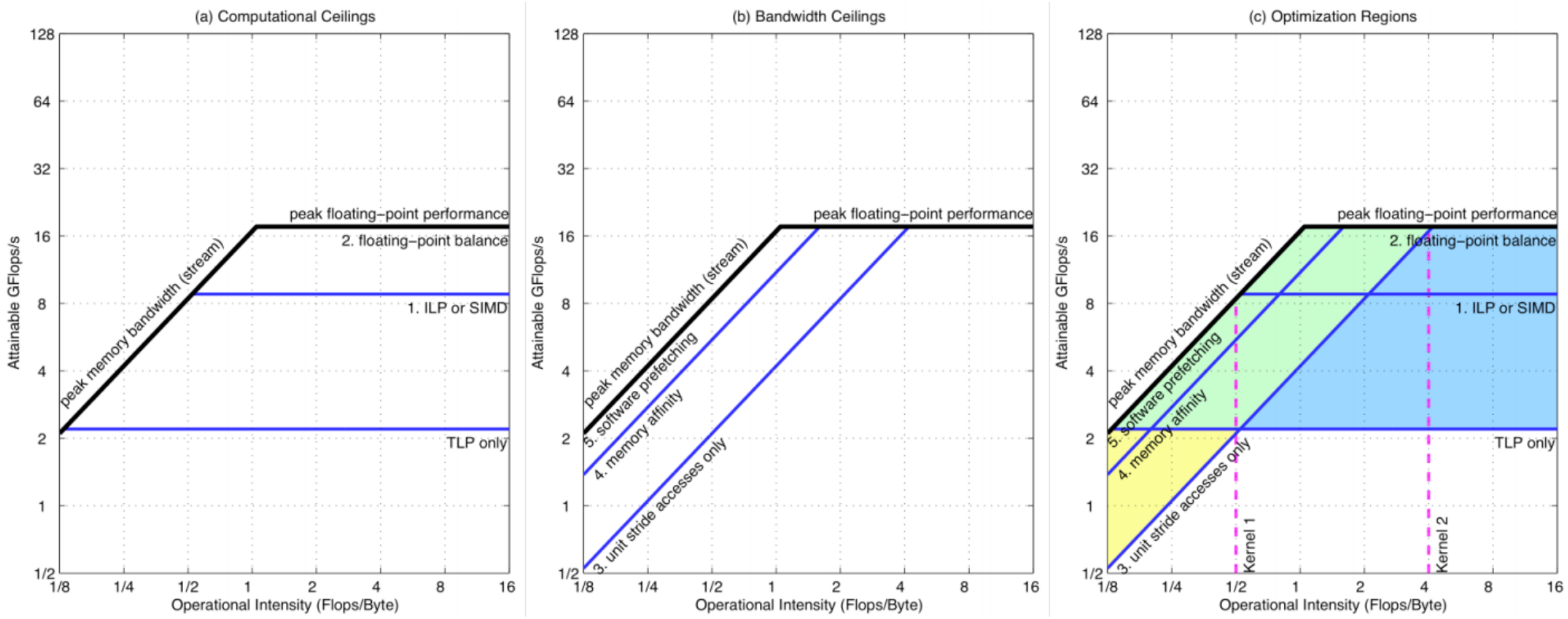

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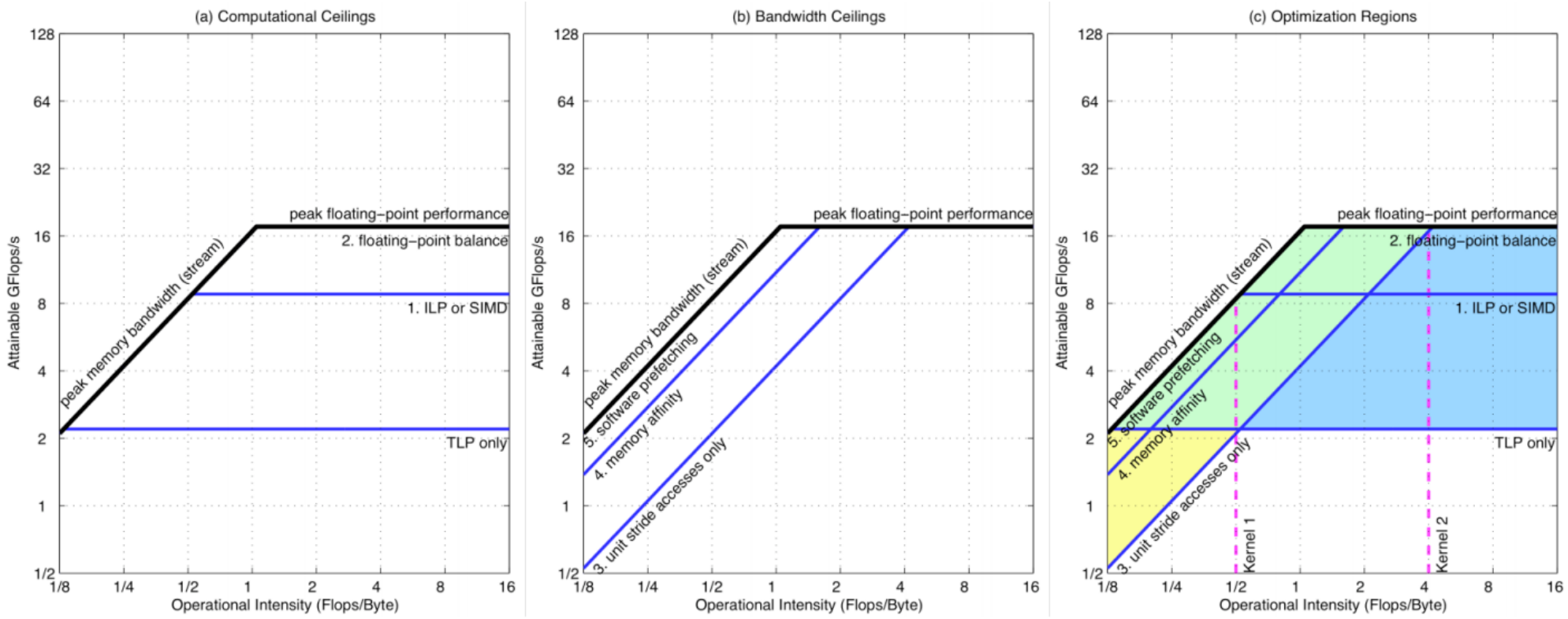

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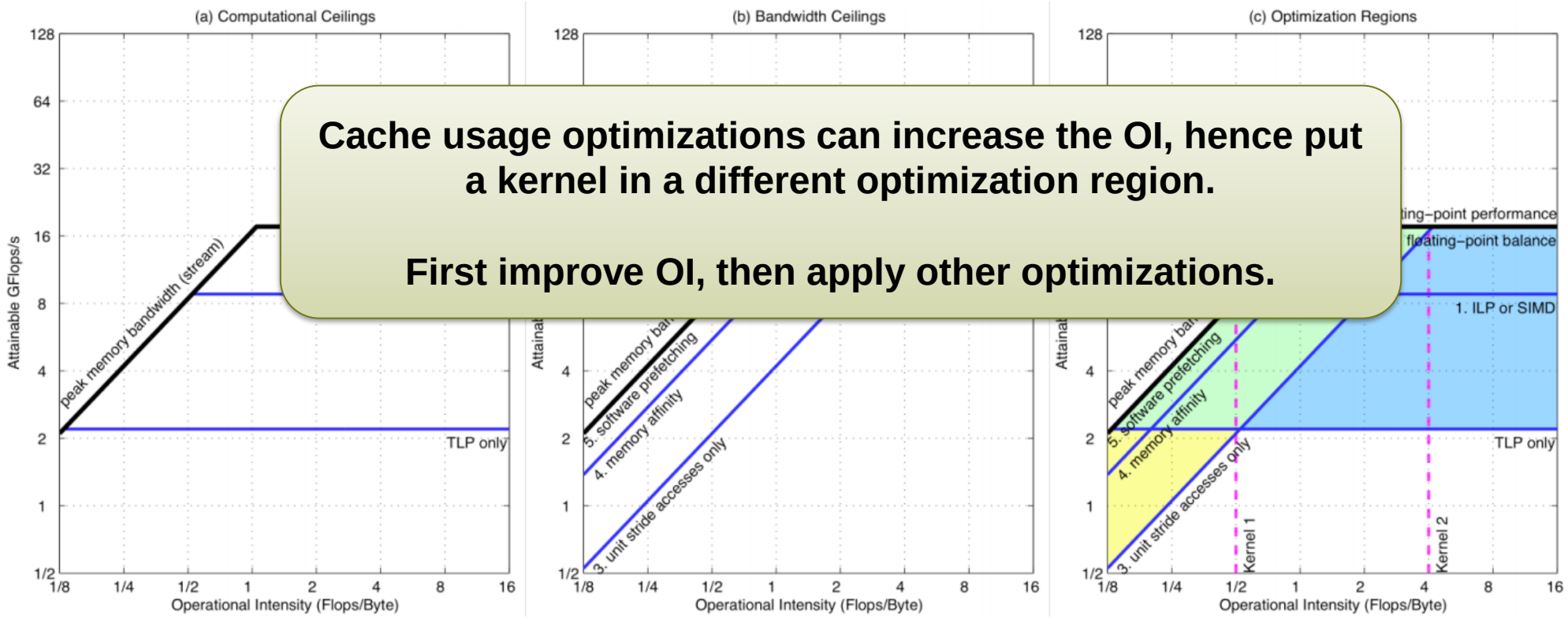

Cache usage optimizations can increase the OI, hence put a kernel in a different optimization region.

First improve OI, then apply other optimizations.

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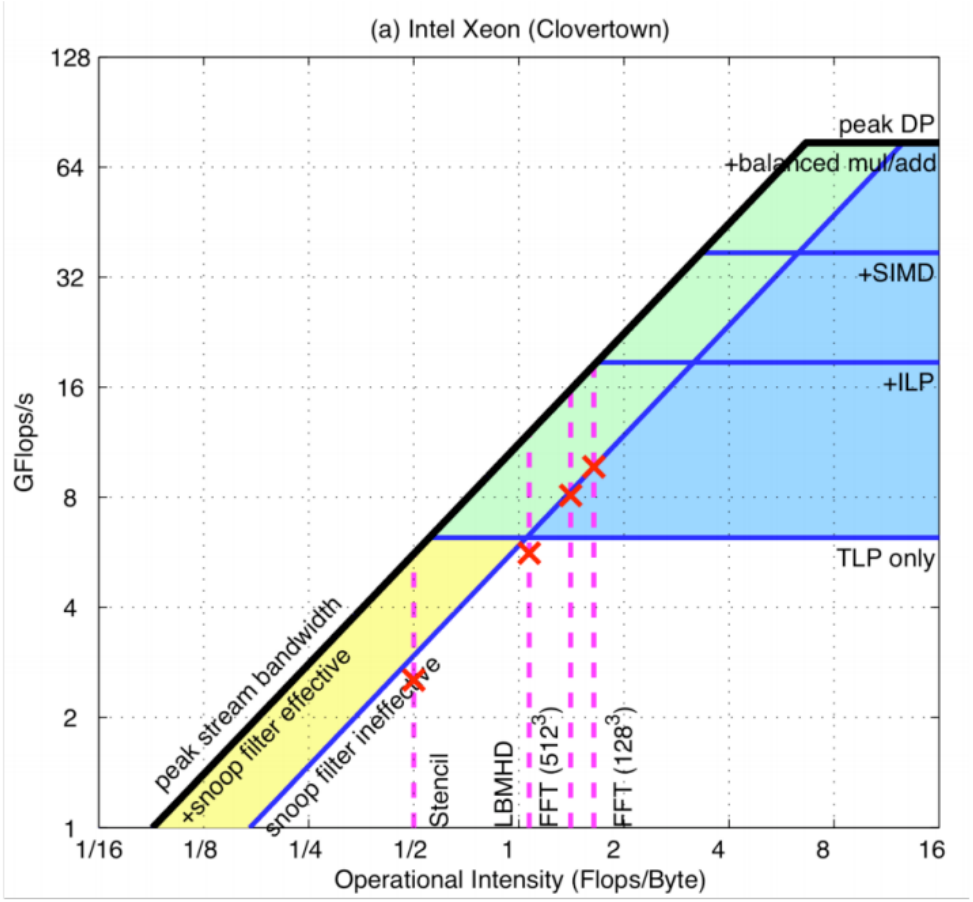
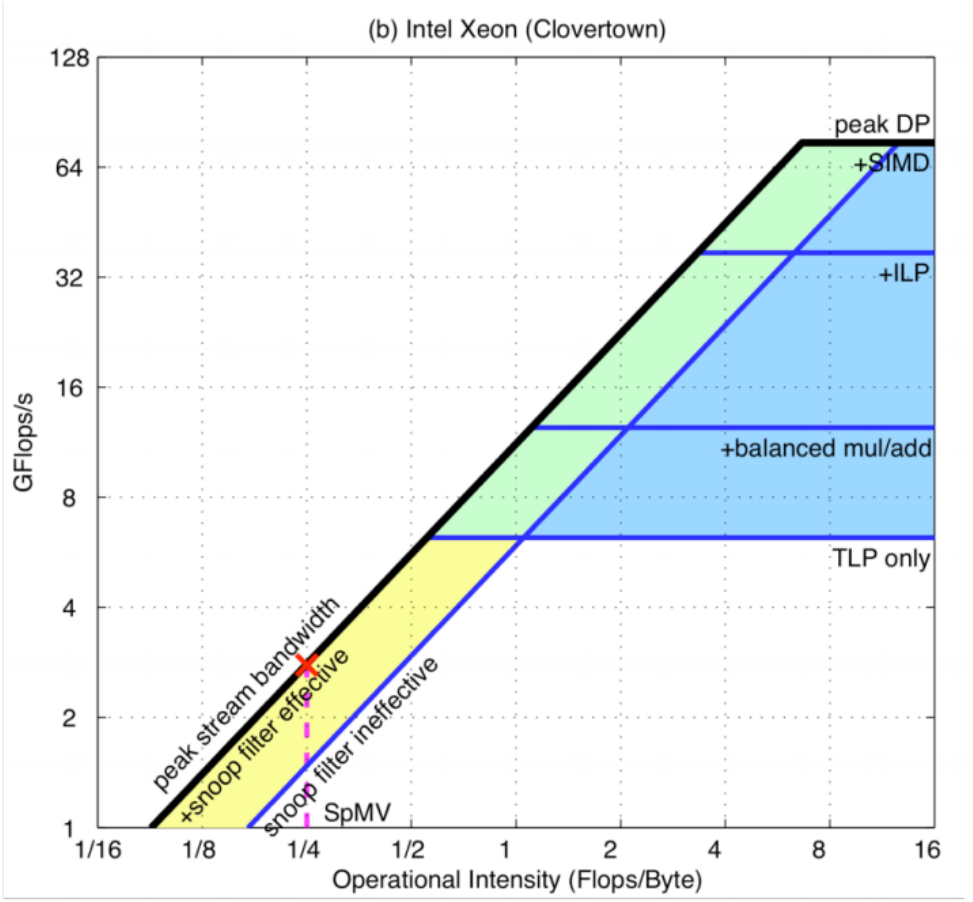
Models & Results





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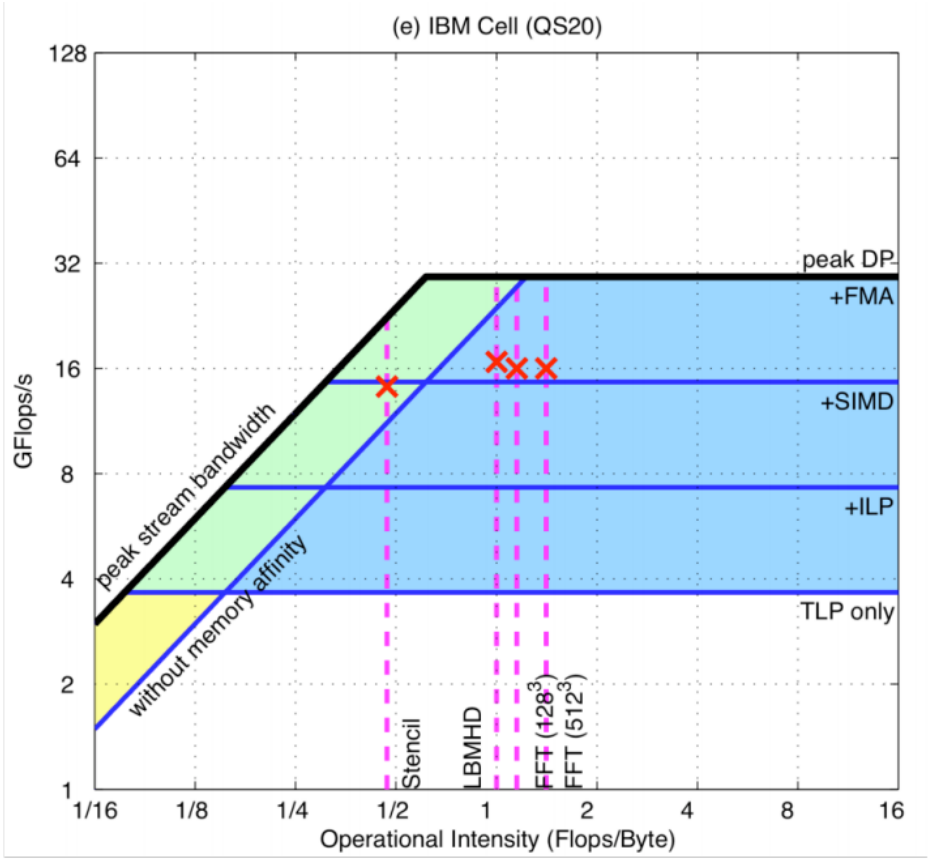

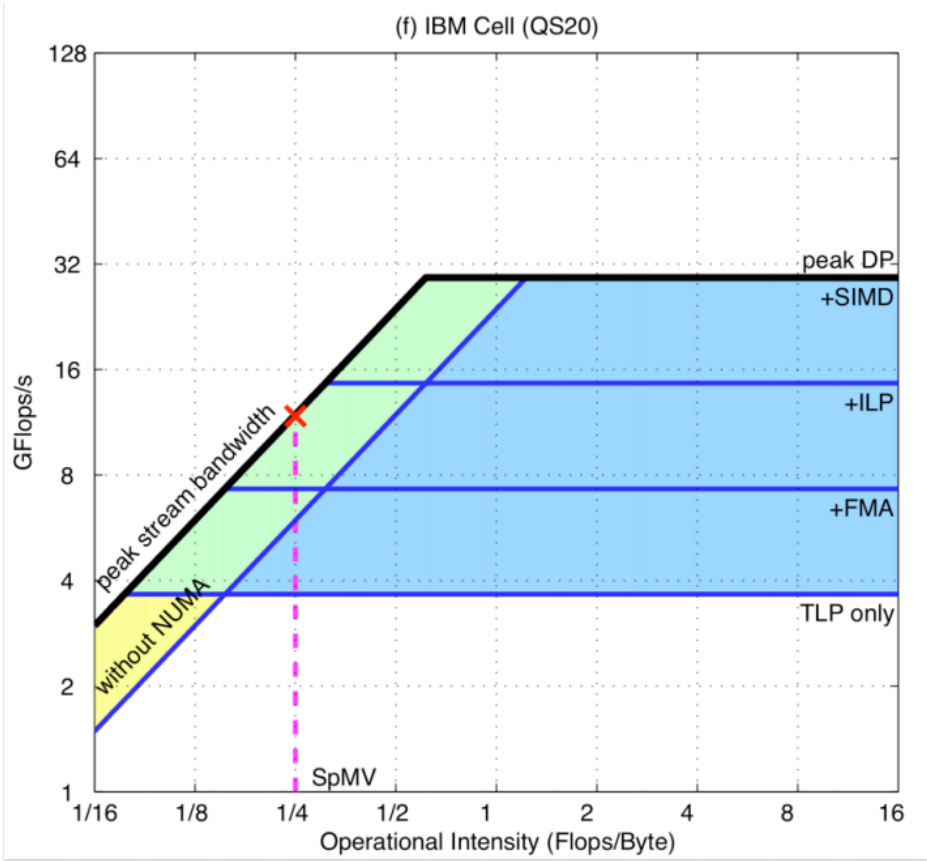

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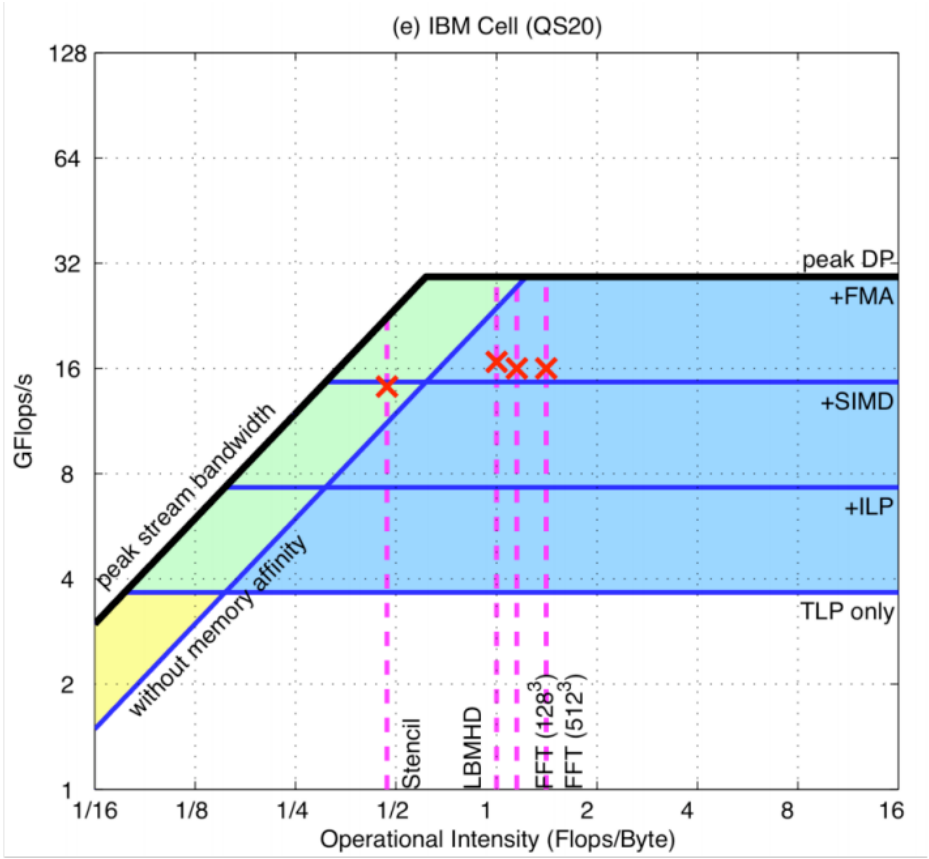
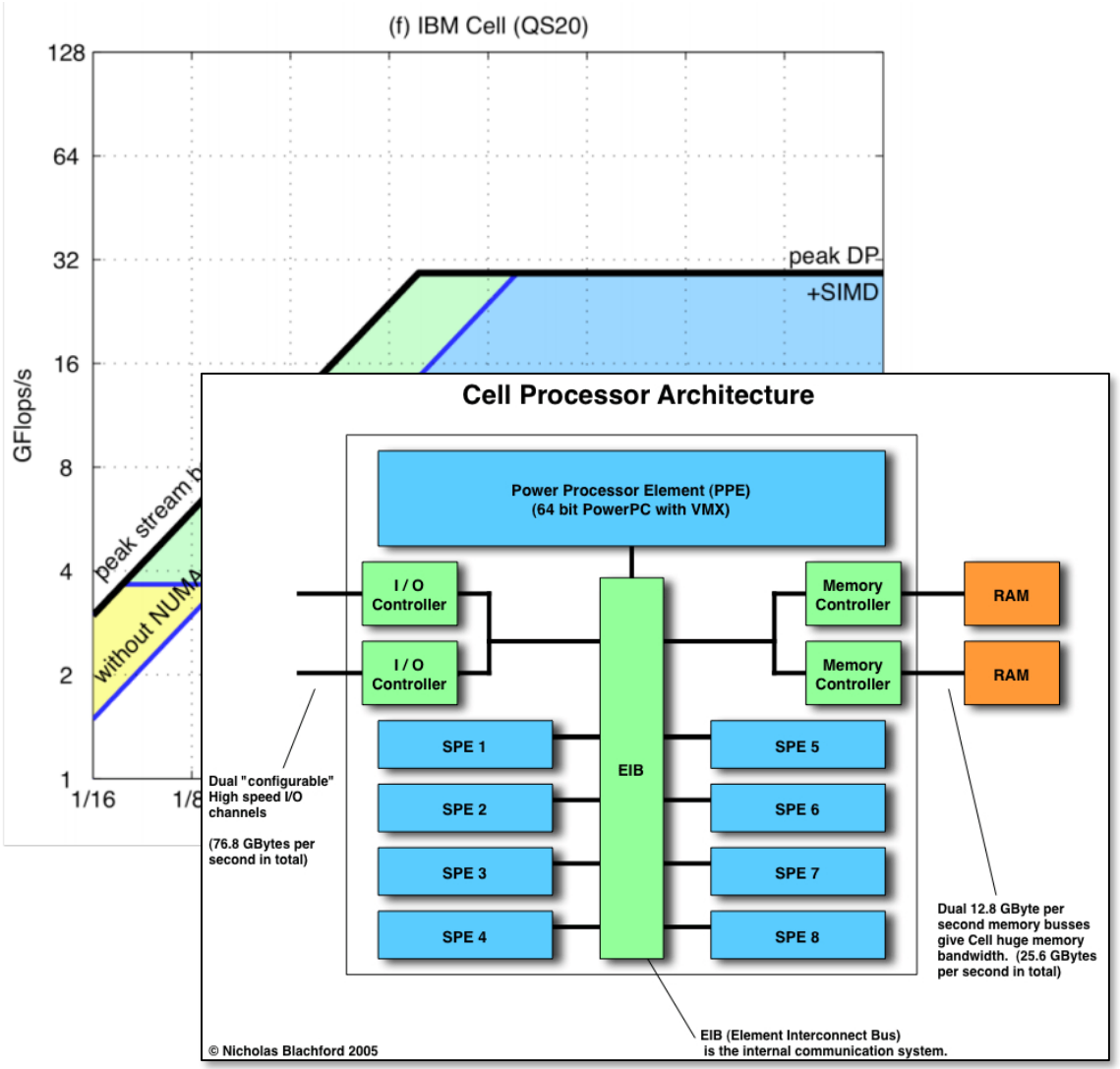
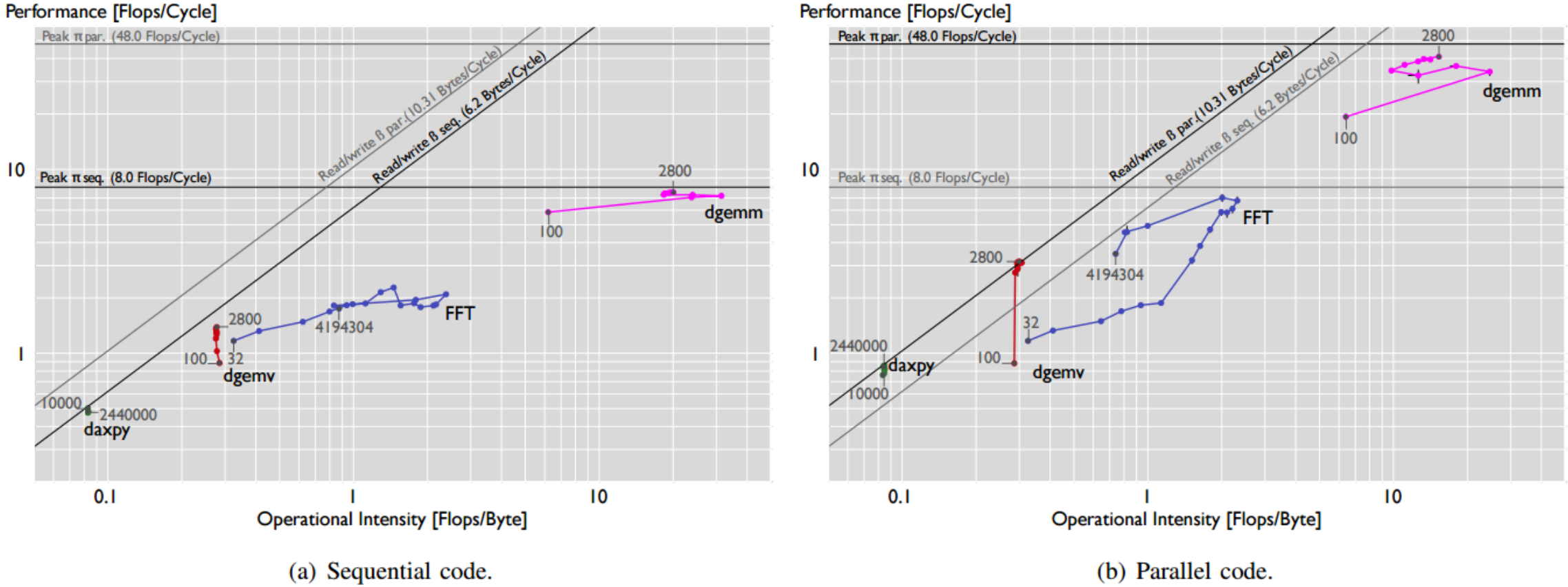




Multithreading



- **The ridge point shifts from 1.3 to 4.6**
- **Increasing the input makes parallelization gain efficiency**
  - Until when the working set gets too big to stay in cache

Ofenbeck, Georg, et al. "Applying the roofline model." Performance Analysis of Systems and Software (ISPASS), 2014 IEEE International Symposium on. IEEE, 2014.

Applying the Roofline Model

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    Counters for floating point operations

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    Read Time Stamp Counter (RDTSC) is still a right choice

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    LLC misses can be an underestimation

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LibLSB: https://spcl.inf.ethz.ch/Research/Performance/LibLSB/

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