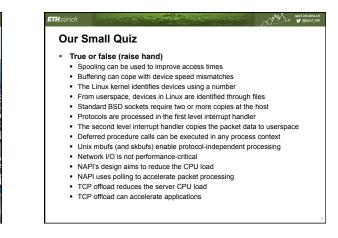
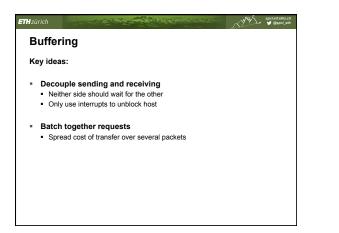
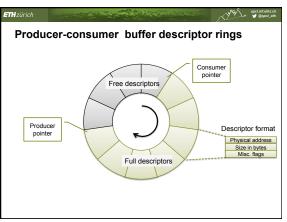
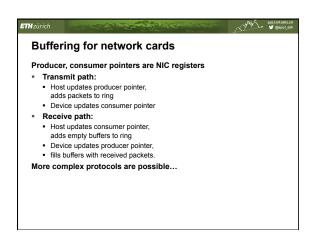
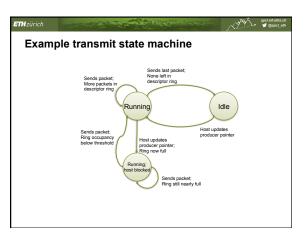
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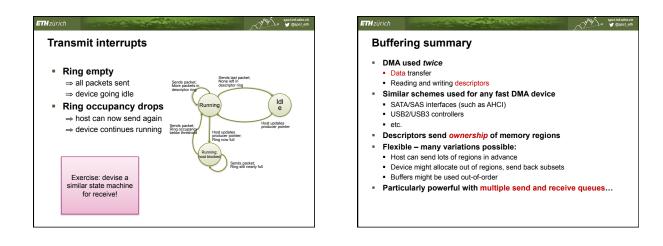


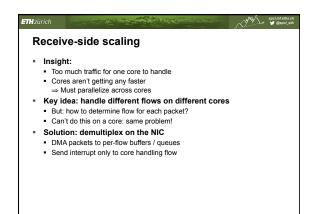


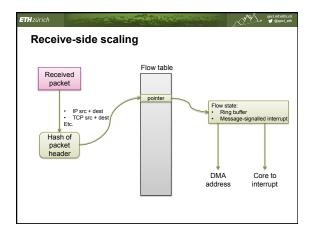


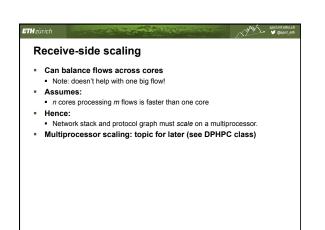




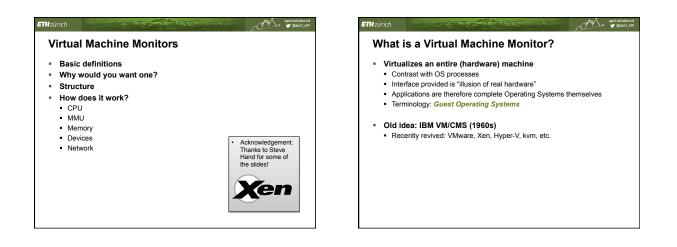


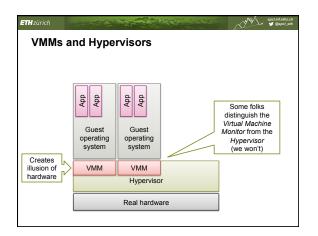


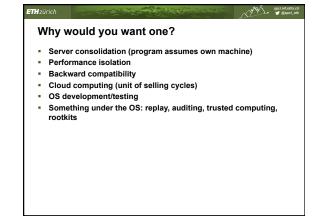


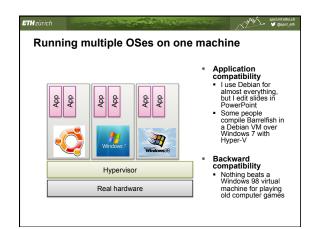


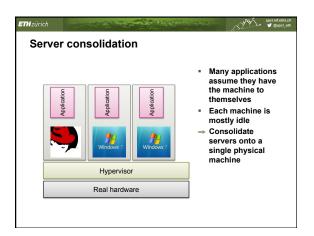


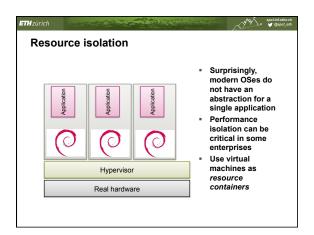


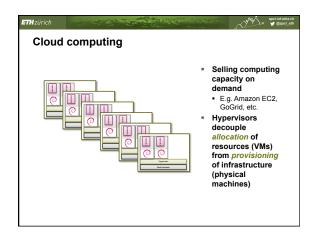


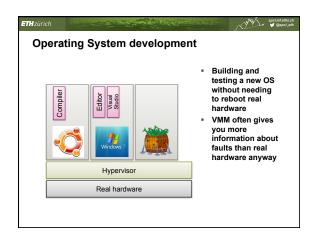


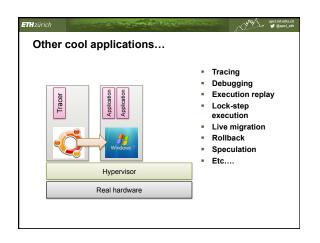


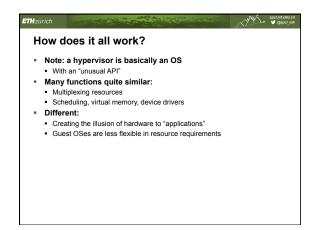


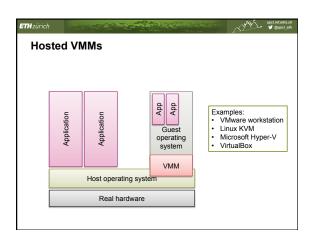












етн <sub>zürich</sub> Нуре	Mzürich Seperies Sepe				
	Console (Mgmt) operating system	ddy Guest operating system	ddy Guest operating system	Examples: • VMware ESX • IBM VM/CMS • Xen	
	VMM	VMM	VMM		
	Hypervisor				
	Real hardware				

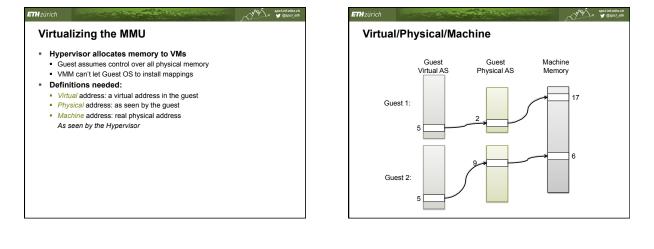
ETH zürich		spcl.inf.ethz.ch y @spcl_eth
How t	o virtualize	
	CPU (s)?	
	/MU?	
-	ical memory?	
	es (disks, etc.)?	
The I	letwork	
and?		

### Hzürich √ spci.int.ethz.ch ✓ generative g **TH**zürich spci.inf.ethz.ch y @spci\_eth Virtualizing the CPU Virtualizing the CPU A CPU architecture is strictly virtualizable if it can be perfectly emulated over itself, with all non-privileged instructions A strictly virtualizable processor can execute a complete native Guest OS executed natively · Guest applications run in user mode as before Guest kernel works exactly as before Privileged instructions ⇒ trap Problem: x86 architecture is not virtualizable 8 Kernel-mode (i.e., the VMM) emulates instruction About 20 instructions are sensitive but not privilegedMostly segment loads and processor flag manipulation · Guest's kernel mode is actually user mode Or another, extra privilege level (such as ring 1) Examples: IBM S/390, Alpha, PowerPC

Non-v	irtualizable x86	: example		
PUSH	/POPF instructions			
<ul> <li>Pu</li> </ul>	h/pop condition code reg	ister		
<ul> <li>Inc</li> </ul>	udes interrupt enable flag	(IF)		
Unpr	vileged instructions:	fine in user space	!	
• IF	is ignored by POPF in use	r mode, not in kernel	mode	
⇒ ∨MM	can't determine if Gue	est OS wants inter	rupts disabled!	
<ul> <li>Ca</li> </ul>	n't cause a trap on a (privi	leged) POPF		
<ul> <li>Pre</li> </ul>	vents correct functioning	of the Guest OS		
	-			

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- Used by, e.g. VMware
- 4. Hardware support: Intel VT-x, AMD-V
  - Extra processor mode causes POPF to trap



### Hzürich spci.inf.ethz.ch y @spci\_eth **MMU Virtualization**

- Critical for performance, challenging to make fast, especially SMP
- Hot-unplug unnecessary virtual CPUs
- Use multicast TLB flush paravirtualizations etc. Xen supports 3 MMU virtualization modes
- 1. Direct ("Writable") pagetables
- 2. Shadow pagetables

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- 3. Hardware Assisted Paging
- OS Paravirtualization compulsory for #1, optional (and very . beneficial) for #2&3

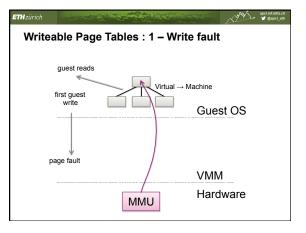
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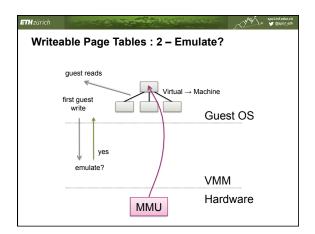
### Paravirtualization approach

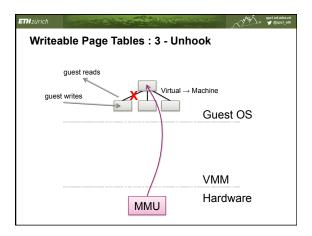
- Guest OS creates page tables the hardware uses
- VMM must validate all updates to page tables
- Requires modifications to Guest OS
- Not quite enough.. VMM must check all writes to PTEs
- · Write-protect all PTEs to the Guest kernel
  - Add a HyperCall to update PTEs
  - Batch updates to avoid trap overhead
  - OS is now aware of machine addresses
  - Significant overhead!

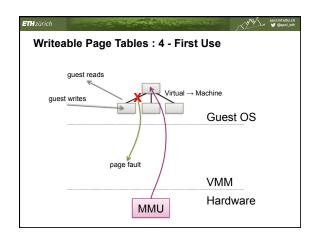
# spci.inf.ethz.cl y @spci\_eth Para-Virtualizing the MMU Guest OSes allocate and manage own PTs Hypercall to change PT base VMM must validate PT updates before use

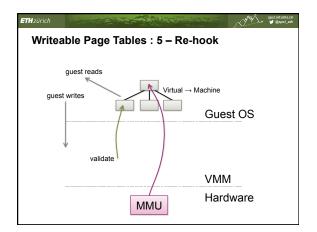
- Allows incremental updates, avoids revalidation
- Validation rules applied to each PTE:
  - 1. Guest may only map pages it owns\* 2. Pagetable pages may only be mapped RO
- VMM traps PTE updates and emulates, or 'unhooks' PTE page for bulk updates

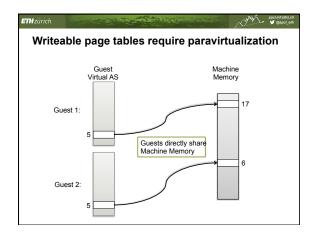






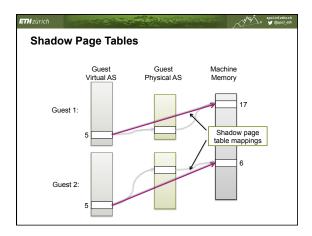


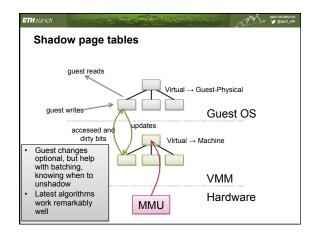




Guest OS sets up its own page tables
Not used by the hardware!
VMM maintains shadow page tables
<ul> <li>Map directly from Guest VAs to Machine Addresses</li> </ul>
<ul> <li>Hardware switched whenever Guest reloads PTBR</li> </ul>
VMM must keep V $\!$
<ul> <li>VMM write-protects all guest page tables</li> </ul>
<ul> <li>Write ⇒ trap: apply write to shadow table as well</li> </ul>
<ul> <li>Significant overhead!</li> </ul>

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### Hardware support

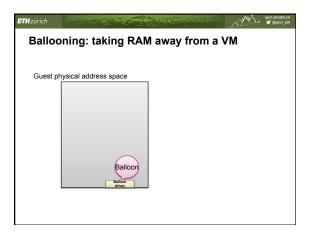
- "Nested page tables"
- Relatively new in AMD (NPT) and Intel (EPT) hardware
- Two-level translation of addresses in the MMU
   Hardware knows about:
  - $V \rightarrow P$  tables (in the Guest)
  - $P \rightarrow M$  tables (in the Hypervisor)
- Tagged TLBs to avoid expensive flush on a VM entry/exit
- Very nice and easy to code to
- One reason kvm is so small
- Significant performance overhead...

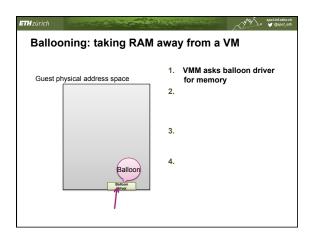
## Memory allocation

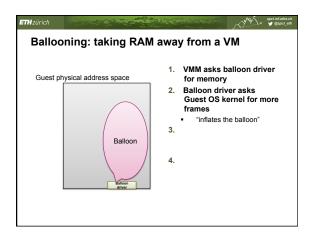
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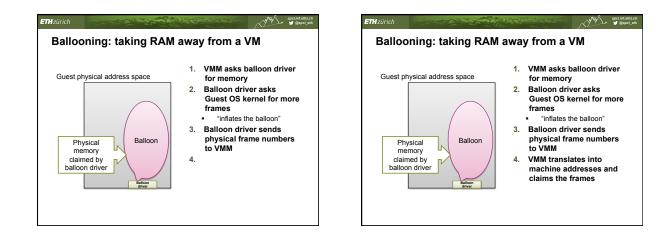
- anooution
- Guest OS is not expecting physical memory to change in size!
- Two problems:
  - Hypervisor wants to overcommit RAMHow to reallocate (machine) memory between VMs
- Phenomenon: Double Paging
- Hypervisor pages out memory
- GuestOS decides to page out physical frame
- (Unwittingly) faults it in via the Hypervisor, only to write it out again

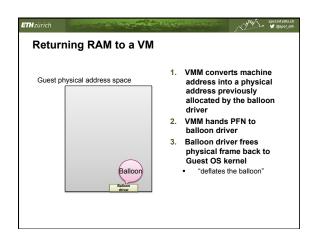
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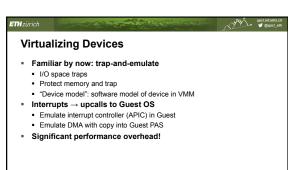










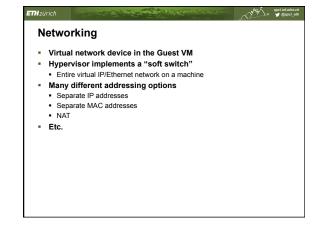


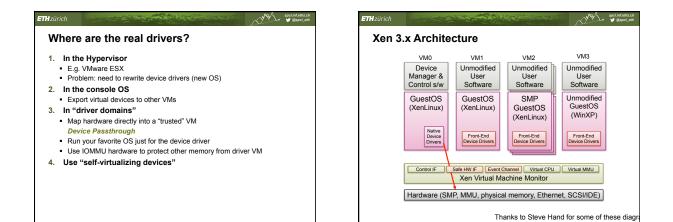
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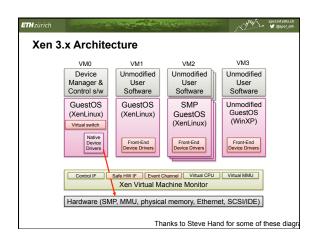
### Paravirtualized devices

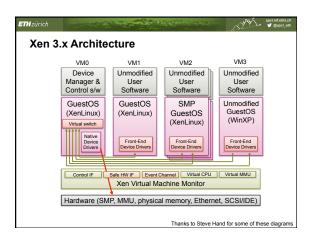
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- "Fake" device drivers which communicate efficiently with VMM via hypercalls
- Used for block devices like disk controllers
   Network interfaces
- "VMware tools" is mostly about these
- Dramatically better performance!

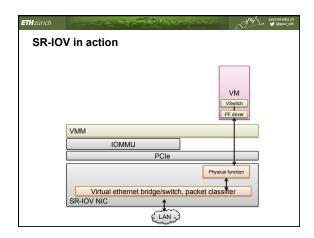


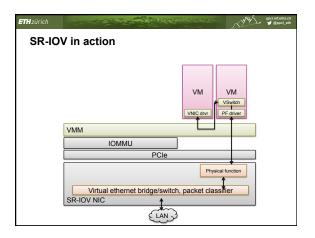


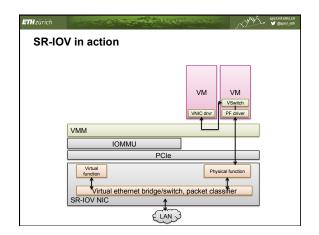


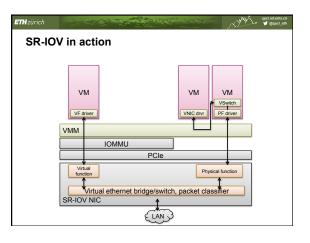


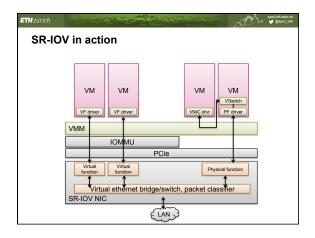












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	VM VM VM VM VM VF driver VF driver VNIC dry PF driver
	IOMMU
	PCle
	Virtual Virtual Virtual Physical function function Virtual ethernet bridge/switch, packet classifier
	SR-IOV NIC
	(LAN)

