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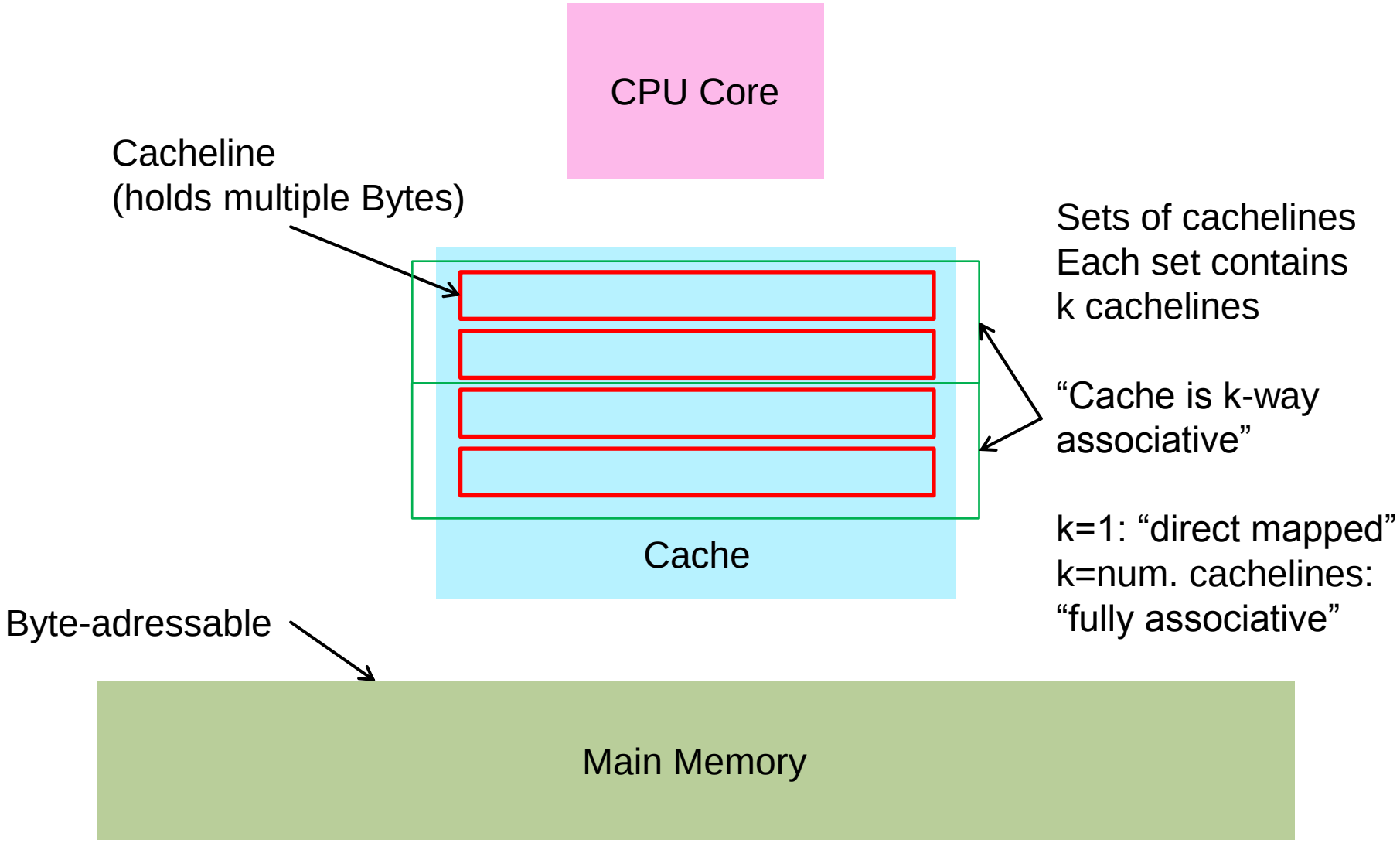
DPHPC Recitation Session 3
Caches

Cache Organization – Cachelines & Sets



Cache Organization – Lookup Procedure

- **How do we check if a memory address X is cached?**
  - Each address can go into exactly one set
  - Split address into three parts: Tag, Set, Offset
  - Use the set part to locate the correct set
  - Compare the tag to all stored tags which are “valid”

Quiz

- **Explain the term**
  - Cache coherence
  - Multi-level cache
  - Shared Cache
  - Write back / write through cache
  - Victim cache

Cache coherence

- **Assume we have two cores, each with its own cache**
- **Both load a shared variable X=0**
- **Now core0 writes to X=1**
- **What happens if core1 uses/reads X now?**

- **What actually happens depends on the cache implementation, i.e., if we have a write back or write through cache**
- **But what we want (cache coherence) is:**
  - Updates are visible to all readers (Write propagation)
  - Writes to the same location appear in order (Write serialization)

Cache Coherence Protocols - MESI

- **Each cacheline is in one of four states**
- **Modifed**
  - The copy in this cache is the only one
  - And the copy in this cache is newer than memory
- **Exclusive**
  - Our cache is the only one which has this cacheline
  - And Memory is up to date
- **Shared**
  - Other copies might exist
  - And memory is up to date
- **Invalid**
  - Cacheline is invalid

Quiz – MESI Protocol

- **What are the events that affect the state of a cache line?**
  - Local Read, Local Write, Read Request on Bus, Shared Signal on Bus, ReadExclusive Request on the Bus
- **What happens if a CL is in state M and the local core reads it?**
  - It stays in state M
- **What happens if a CL is in state I and the local core reads it?**
  - It goes to state E or S, depending how the other caches respond to the Read Request
- **What happens if a CL is in state I and the local core writes to it**
  - ReadExclusive is used to make sure others invalidate their copy and we can go to state M
- **What happens if a CL is in state M and changes its state?**
  - This happens as a result of a read request, so the CL has to be written to memory first
- **Explain a possible optimization of the MESI protocol**
  - MOESI, allows cache to cache data transfer of modified cache lines

Homework

- Available on course website
- Idea: Solve it after the recitation session
- We discuss the solution briefly next recitation session, good idea to bring your solution to compare and ask questions in case you got different results.