

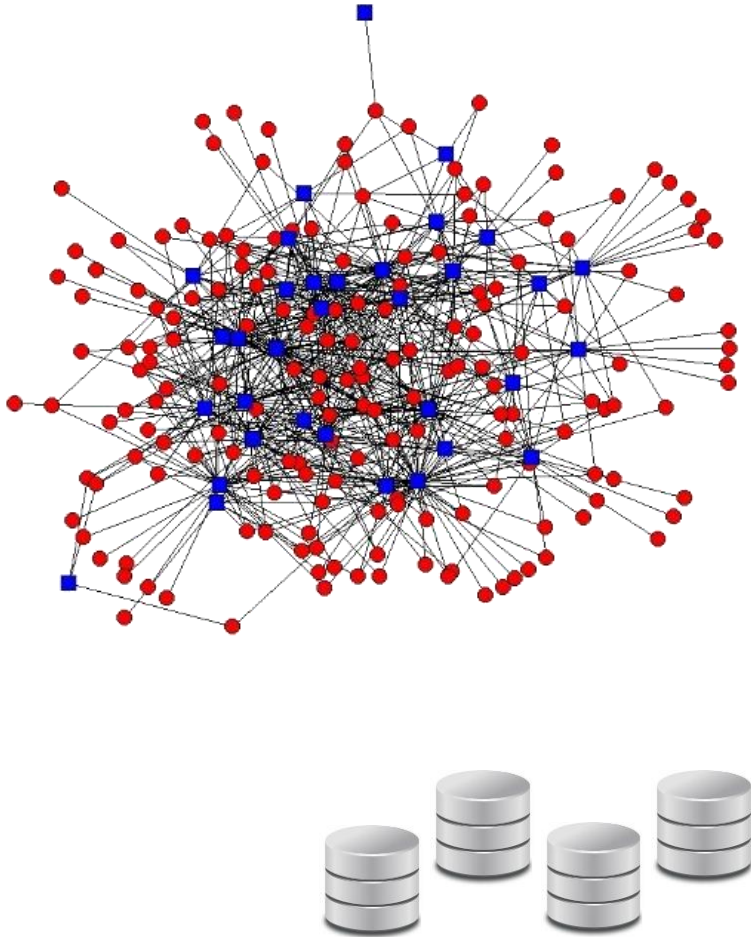
High-Performance Distributed RMA Locks

PATRICK SCHMID, MACIEJ BESTA, TORSTEN HOEFLER

Presented at ARM Research, Austin, Texas, USA, Feb. 2017



NEED FOR EFFICIENT LARGE-SCALE SYNCHRONIZATION



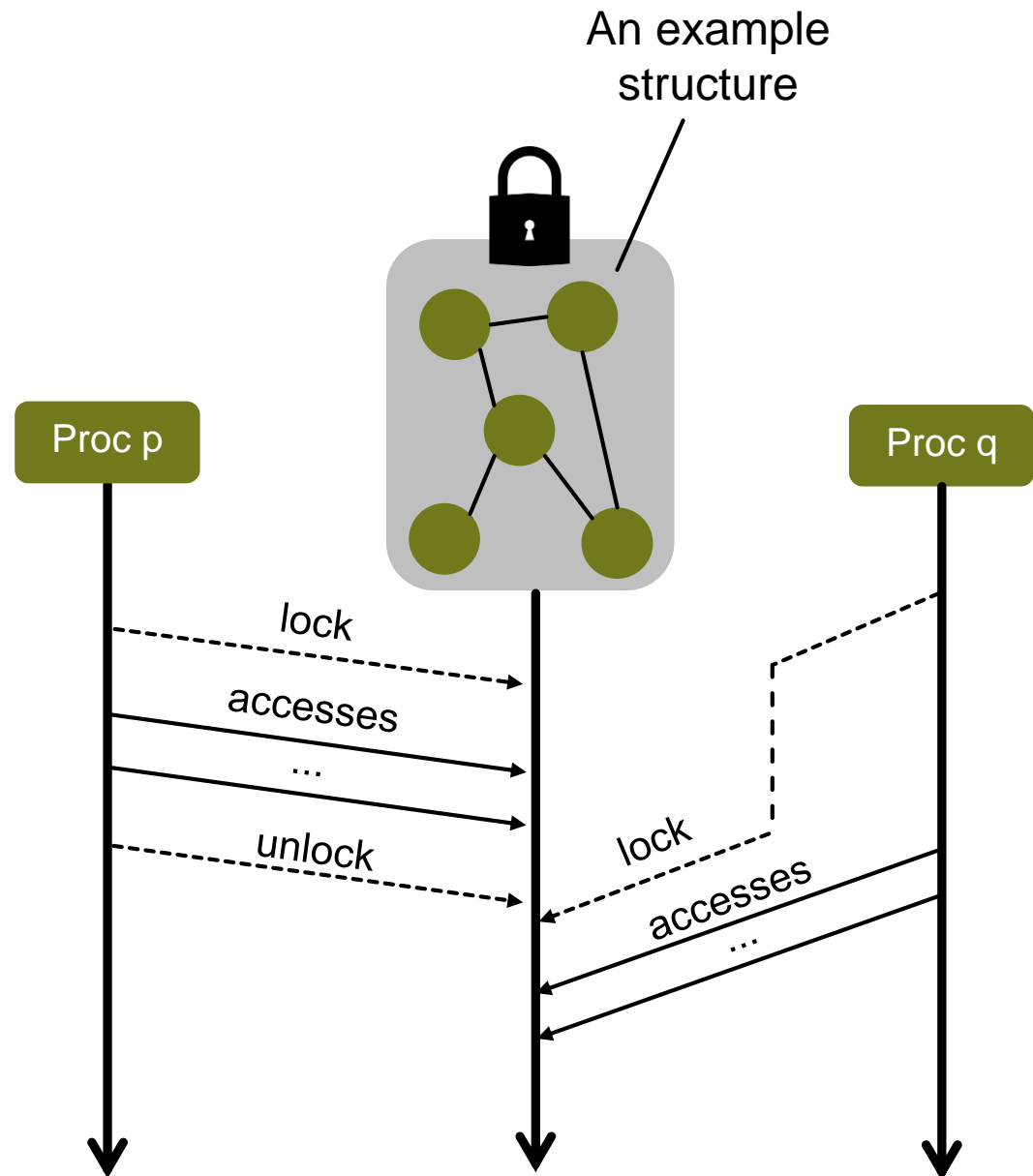
LOCKS



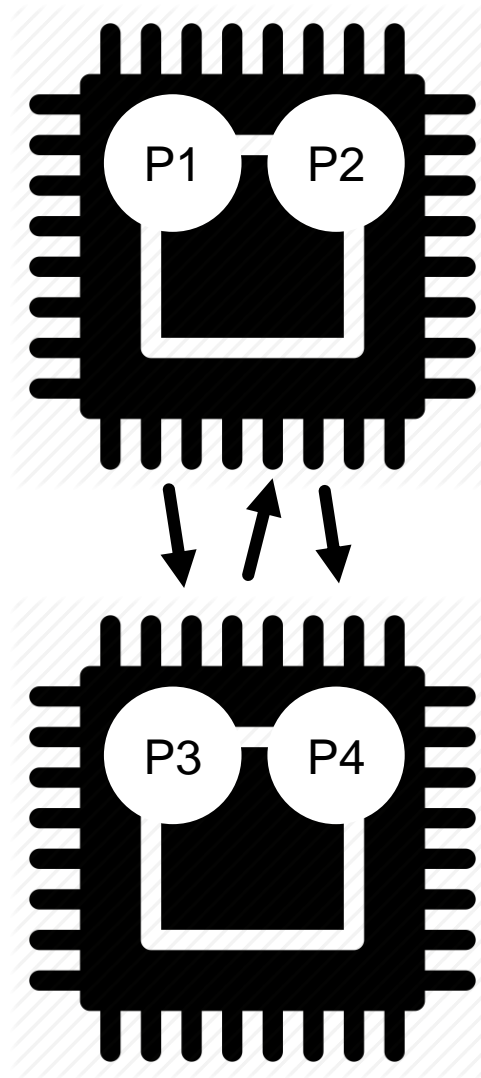
Inuitive semantics




Various performance penalties



LOCKS: CHALLENGES



LOCKS: CHALLENGES



! We need intra- and inter-node topology-awareness

! We need to cover arbitrary topologies

LOCKS: CHALLENGES



We need to distinguish
between readers and writers

Reader

Reader

Reader

Writer



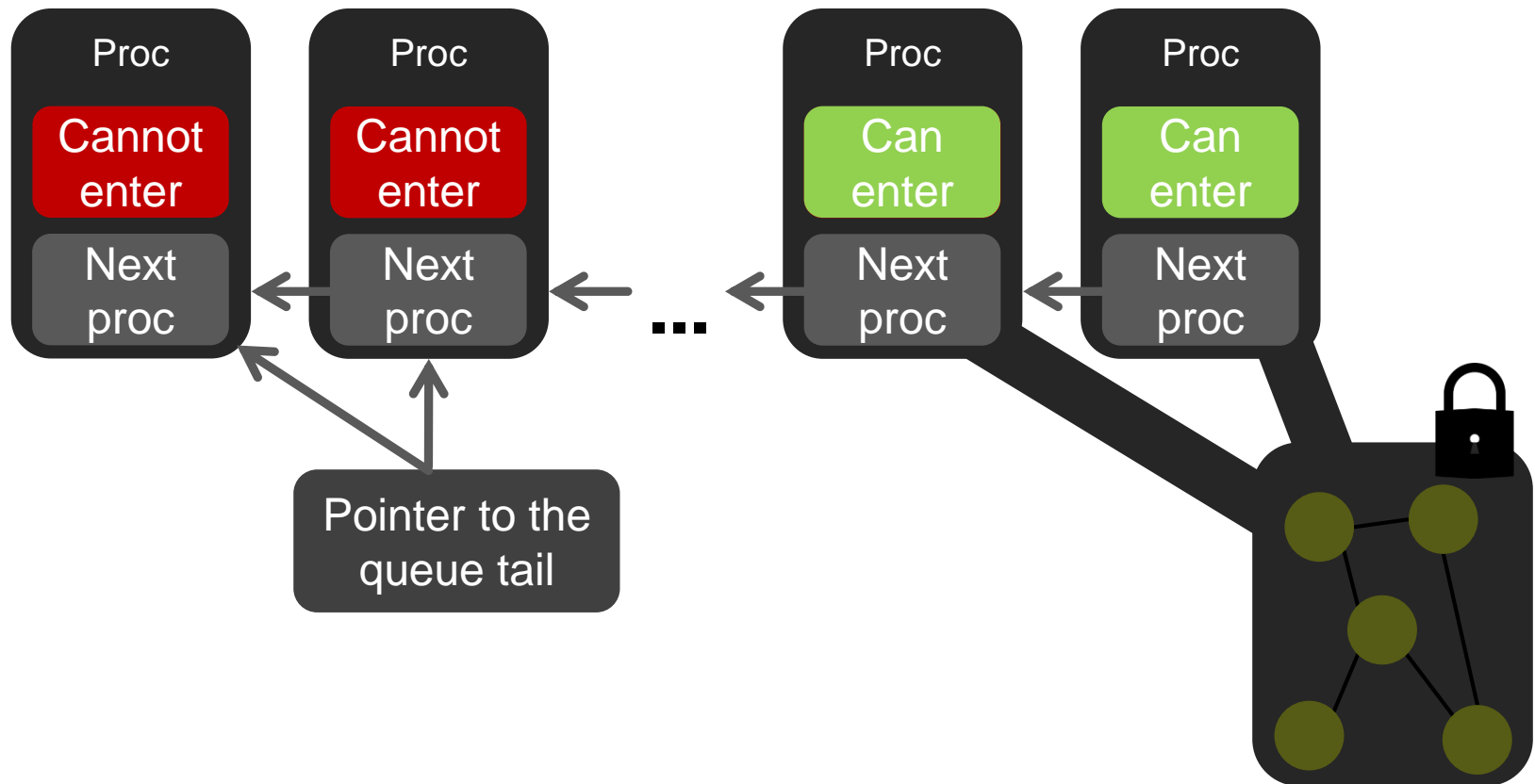
We need flexible
performance for both types
of processes



What will we use in the design?

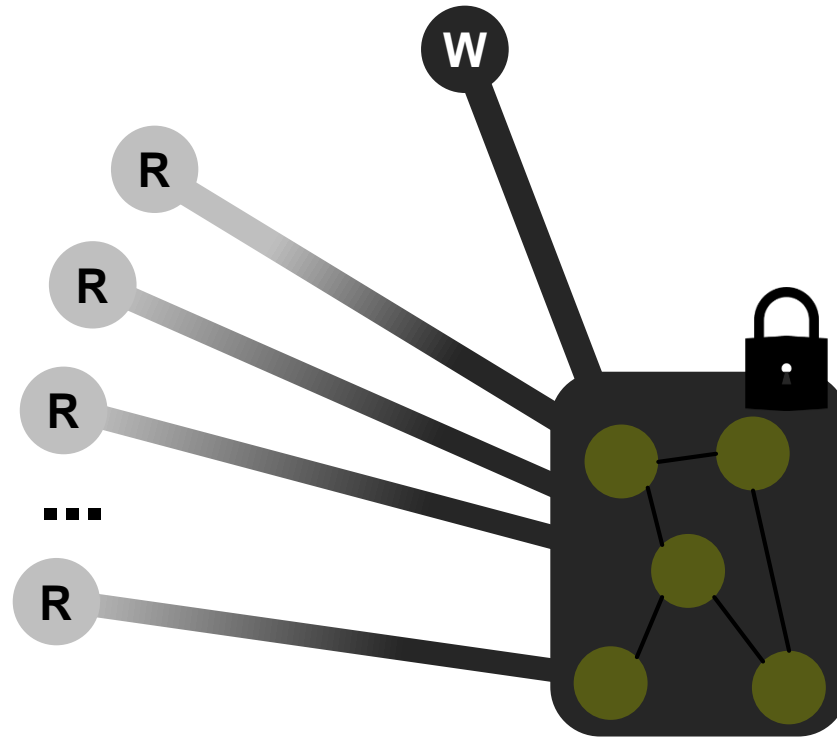
WHAT WE WILL USE

MCS Locks



WHAT WE WILL USE

Reader-Writer Locks





How to manage the design complexity?

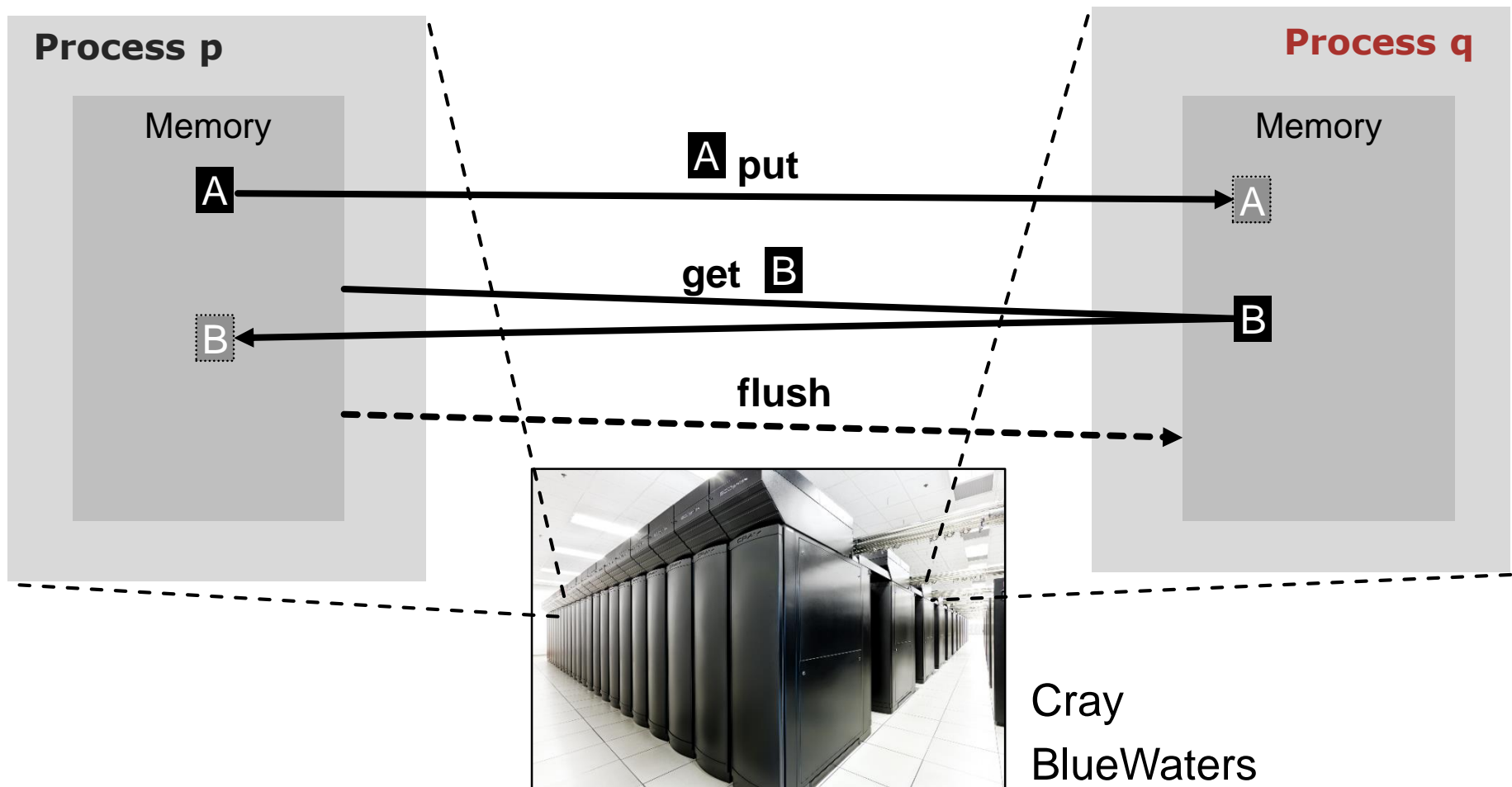


How to ensure tunable performance?



What mechanism to use for efficient implementation?

REMOTE MEMORY ACCESS (RMA) PROGRAMMING



REMOTE MEMORY ACCESS PROGRAMMING

- Implemented in hardware in NICs in the majority of HPC networks (RDMA support).





How to manage the design complexity?



How to ensure tunable performance?



What mechanism to use for efficient implementation?

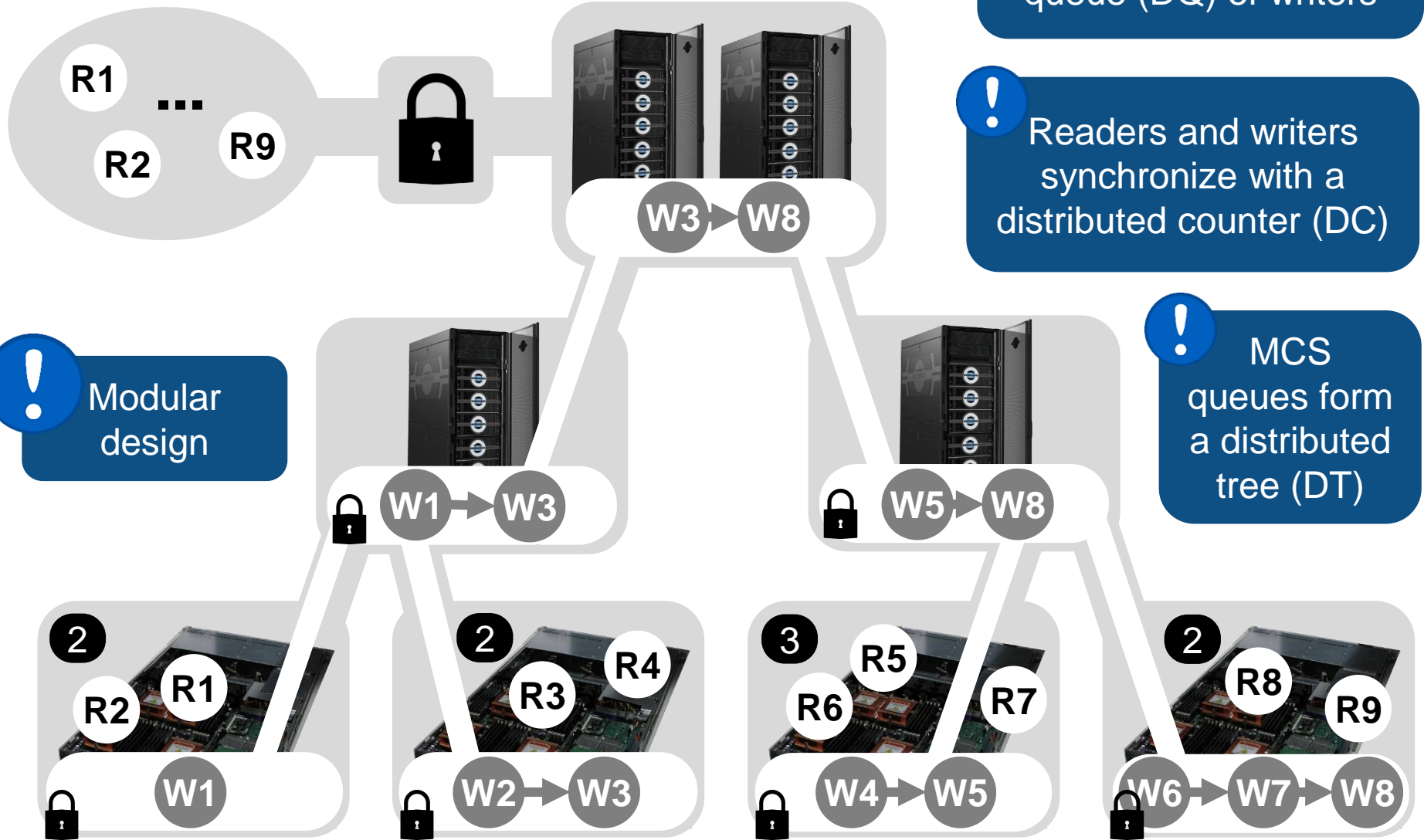
? How to manage the design complexity?

! Each element has its own distributed MCS queue (DQ) of writers

! Readers and writers synchronize with a distributed counter (DC)

! MCS queues form a distributed tree (DT)

! Modular design

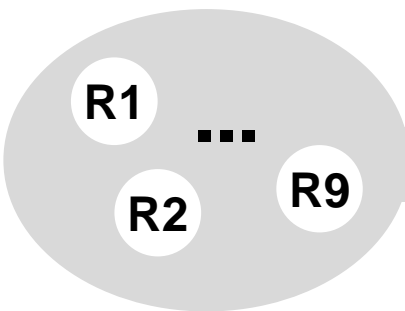


How to ensure tunable performance?

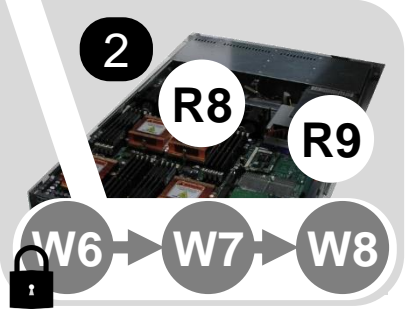
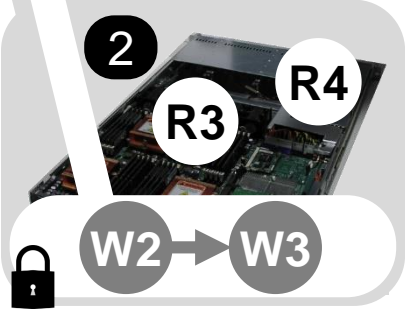
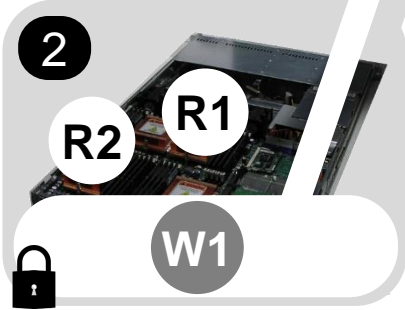
! Each DQ: fairness vs throughput of writers

! DC: a parameter for the latency of readers vs writers

! DT: a parameter for the throughput of readers vs writers



! A tradeoff parameter for every structure



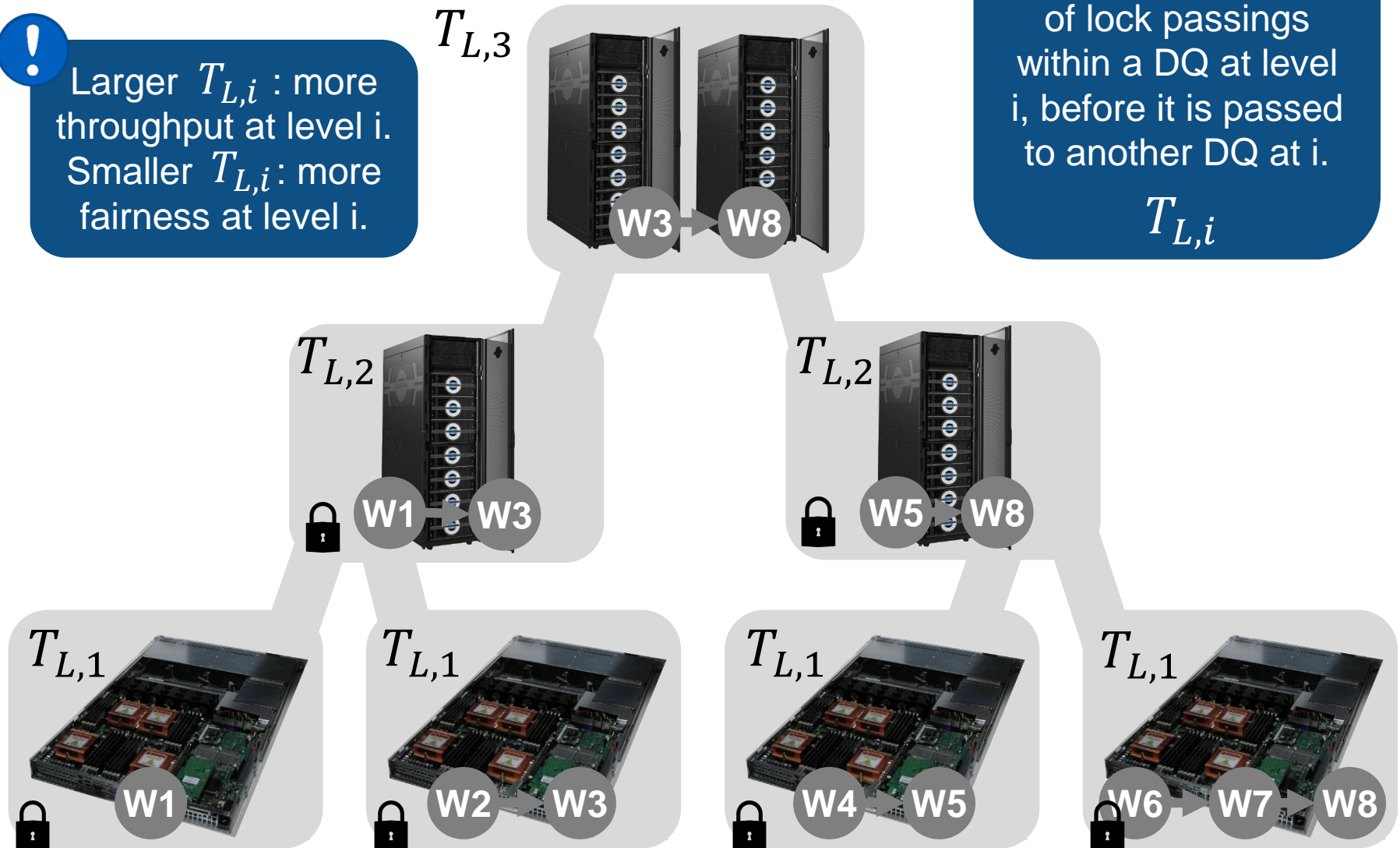
DISTRIBUTED MCS QUEUES (DQs)

Throughput vs Fairness

! Larger $T_{L,i}$: more throughput at level i .
 Smaller $T_{L,i}$: more fairness at level i .

! Each DQ: The maximum number of lock passings within a DQ at level i , before it is passed to another DQ at i .

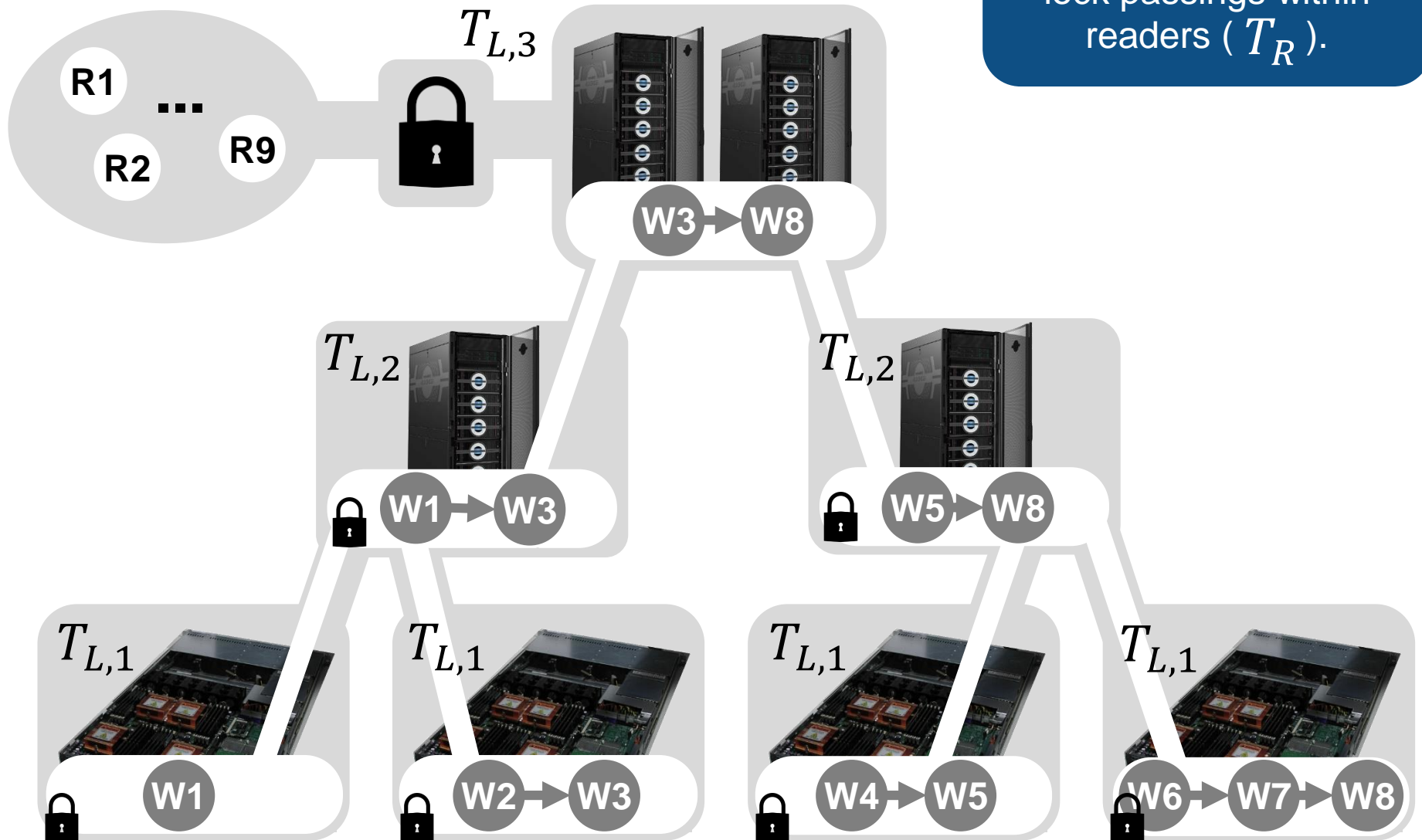
$T_{L,i}$



DISTRIBUTED TREE OF QUEUES (DT)

Throughput of readers vs writers

! DT: The maximum number of consecutive lock passings within readers (T_R).



DISTRIBUTED COUNTER (DC)

Latency of readers vs writers

DC: every k th compute node hosts a partial counter, all of which constitute the DC.

$k = T_{DC}$

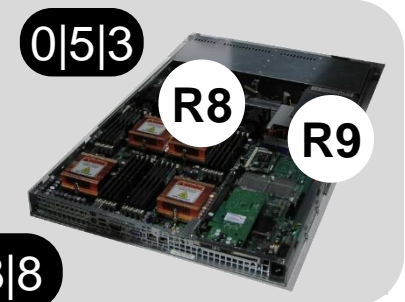
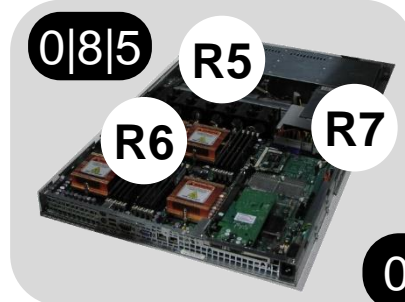
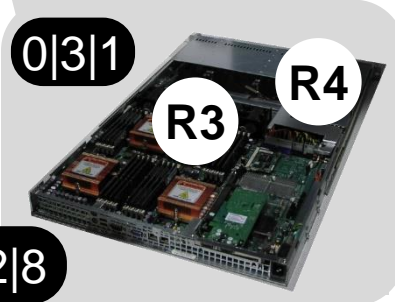
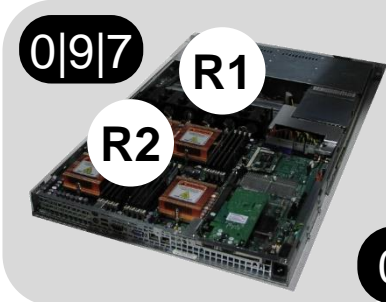


A writer holds the lock $b|x|y$

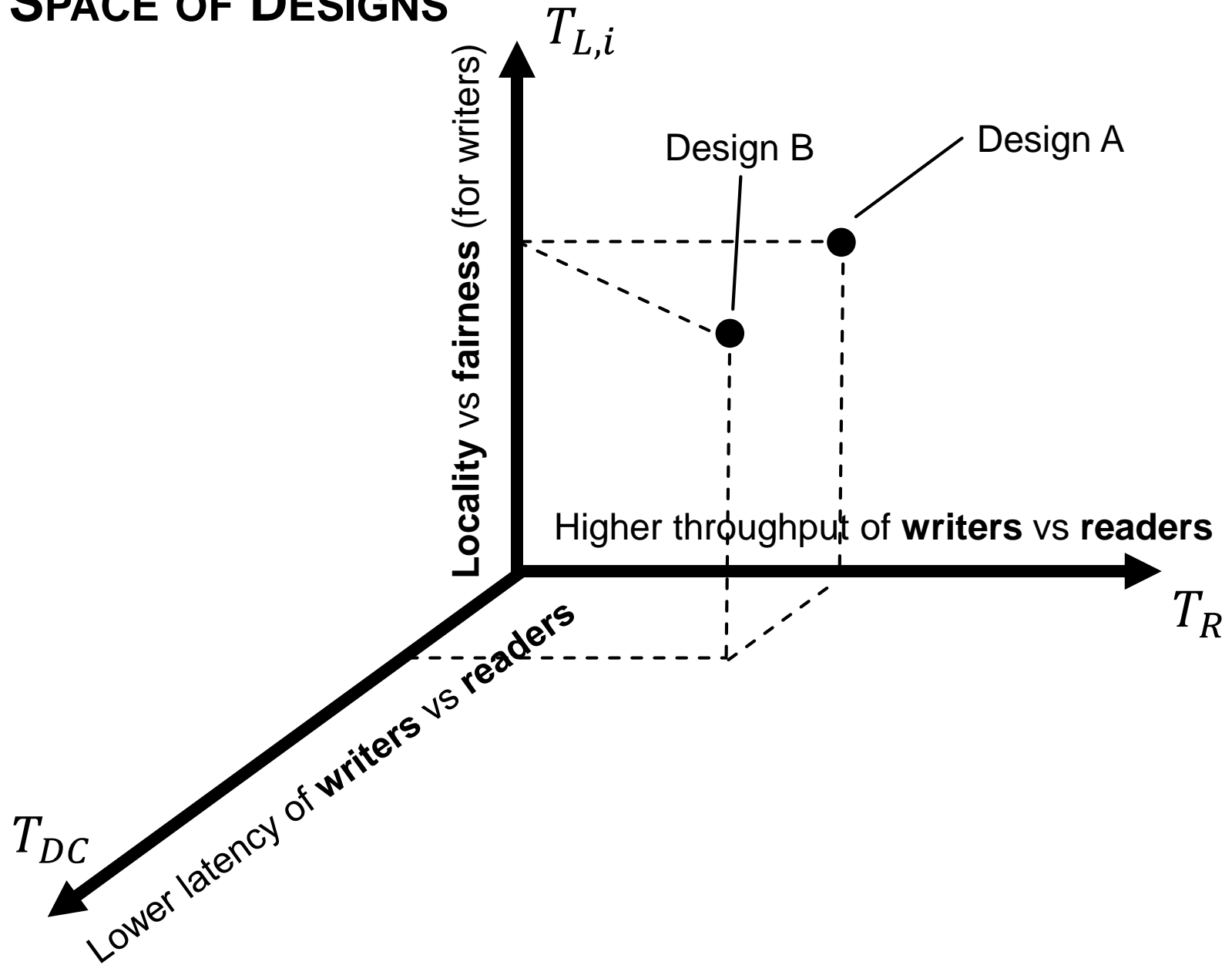
Readers that arrived at the CS

Readers that left the CS

$T_{DC} = 1$
 $T_{DC} = 2$

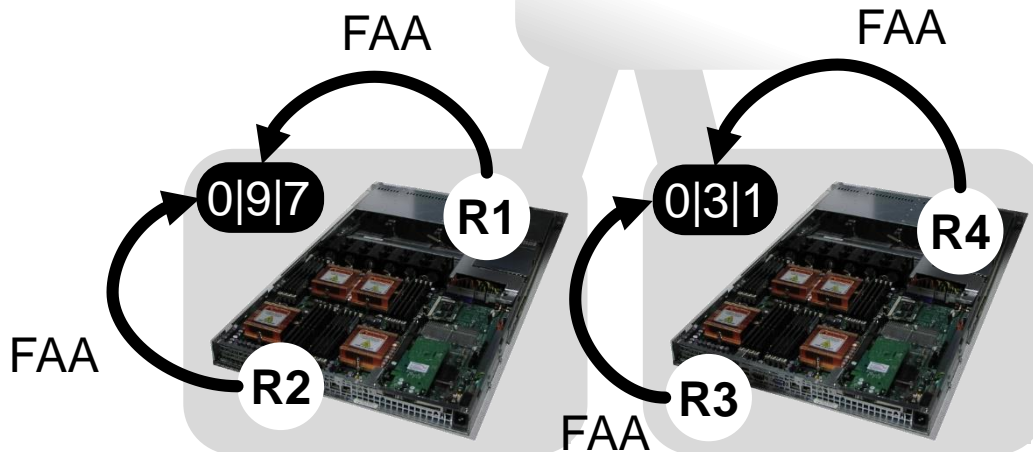


THE SPACE OF DESIGNS



LOCK ACQUIRE BY READERS

! A lightweight acquire protocol for readers: only one atomic fetch-and-add (FAA) operation

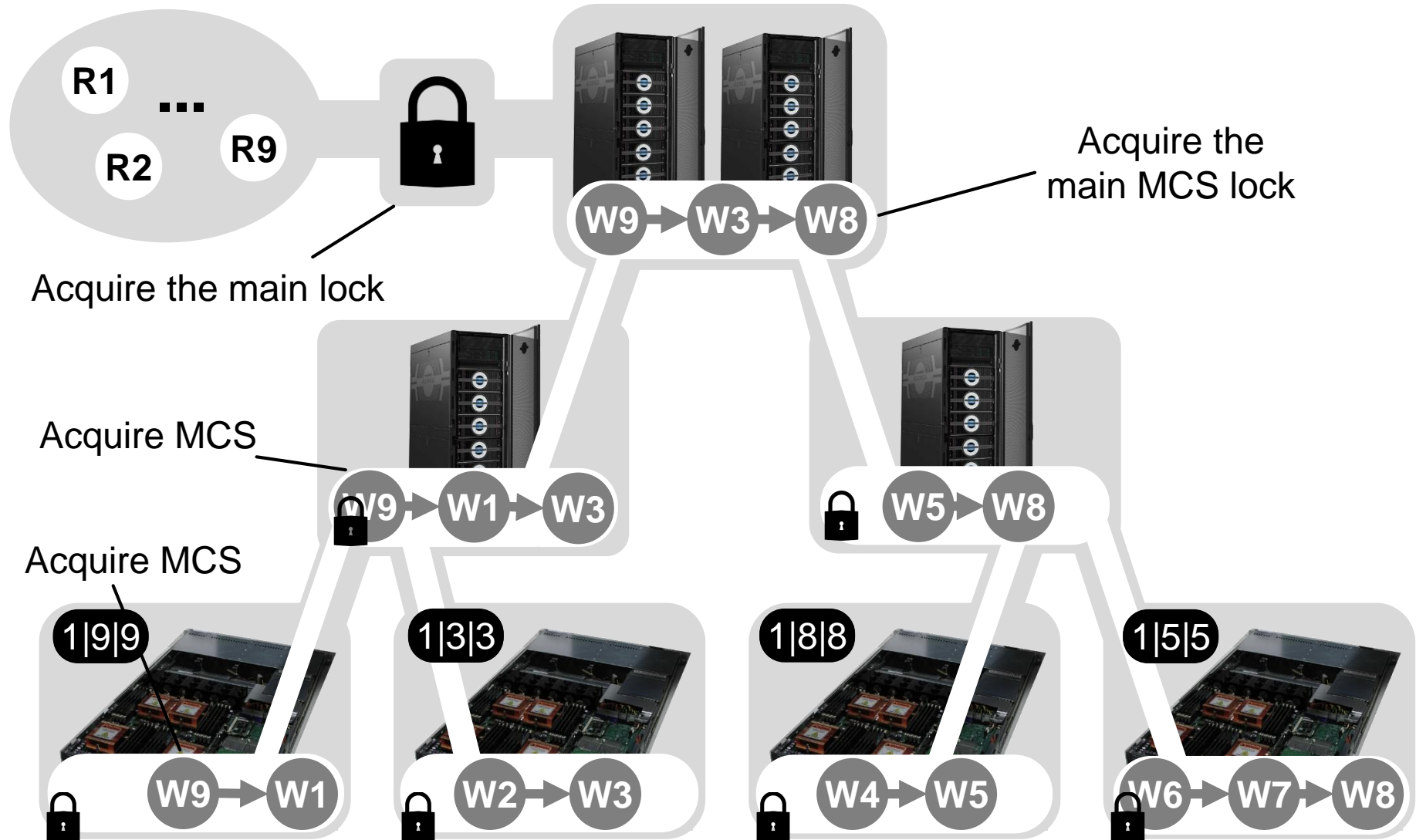


A writer holds the lock — **b|x|y**

Readers that arrived at the CS — **b|x|y**

Readers that left the CS — **b|x|y**

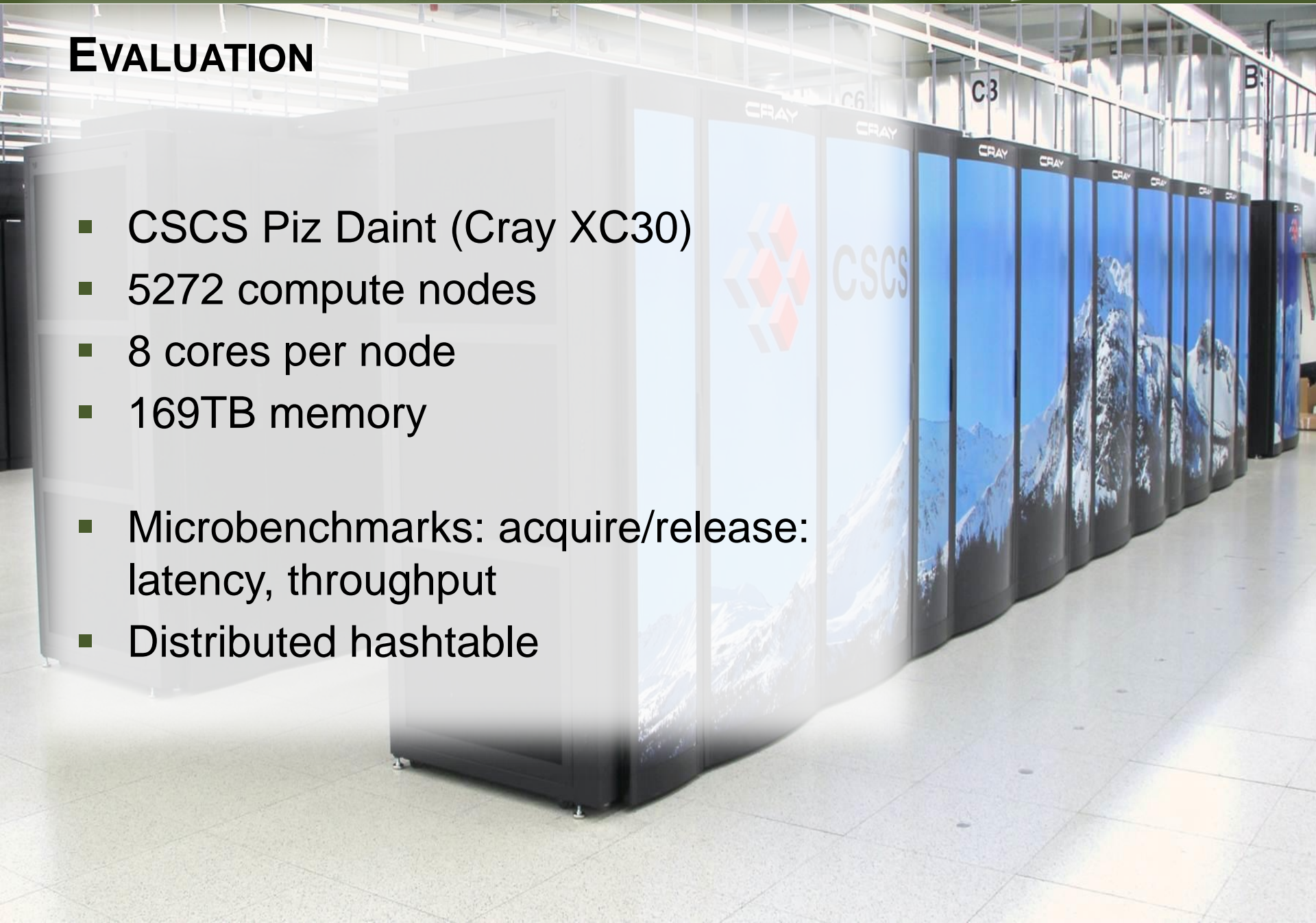
LOCK ACQUIRE BY WRITERS



EVALUATION

- CSCS Piz Daint (Cray XC30)
- 5272 compute nodes
- 8 cores per node
- 169TB memory

- Microbenchmarks: acquire/release:
latency, throughput
- Distributed hashtable



EVALUATION

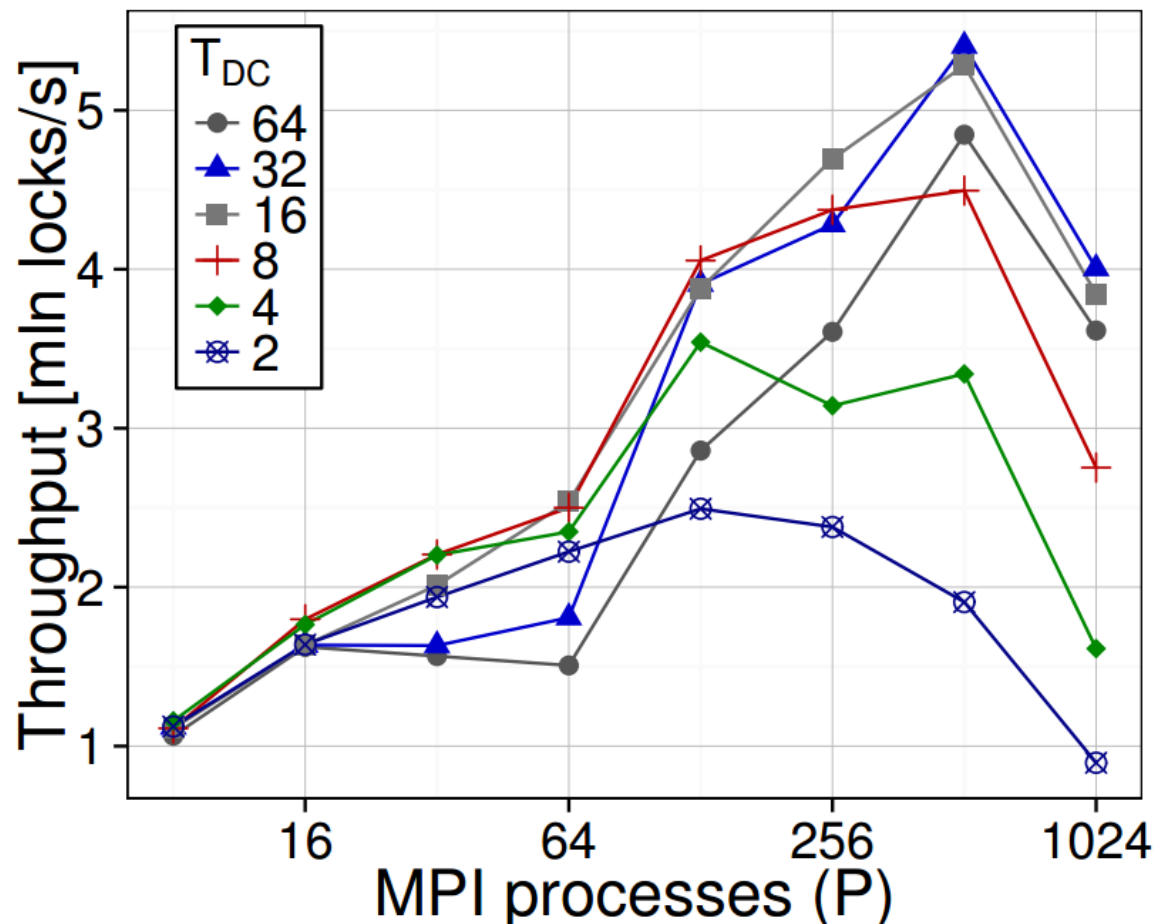
DISTRIBUTED COUNTER ANALYSIS

0|9|7

0|3|1

0|12|8

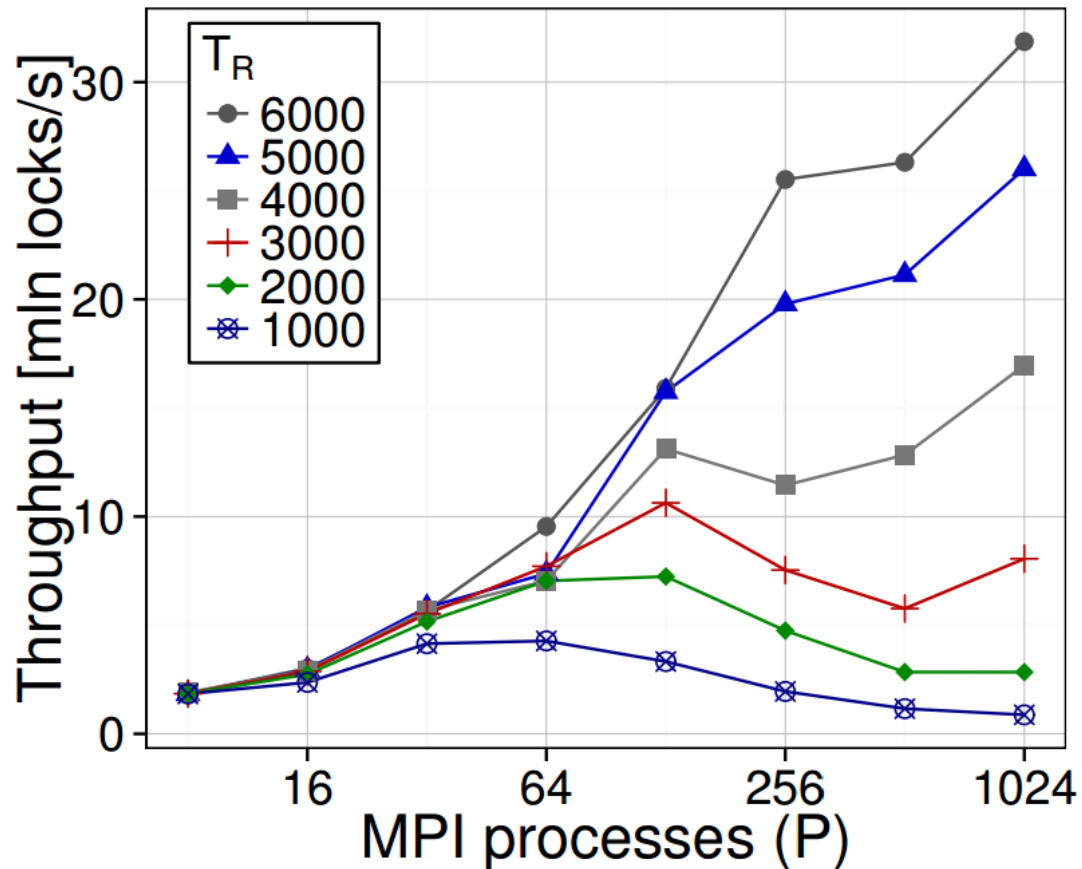
Throughput, 2% writers
Single-operation benchmark



EVALUATION

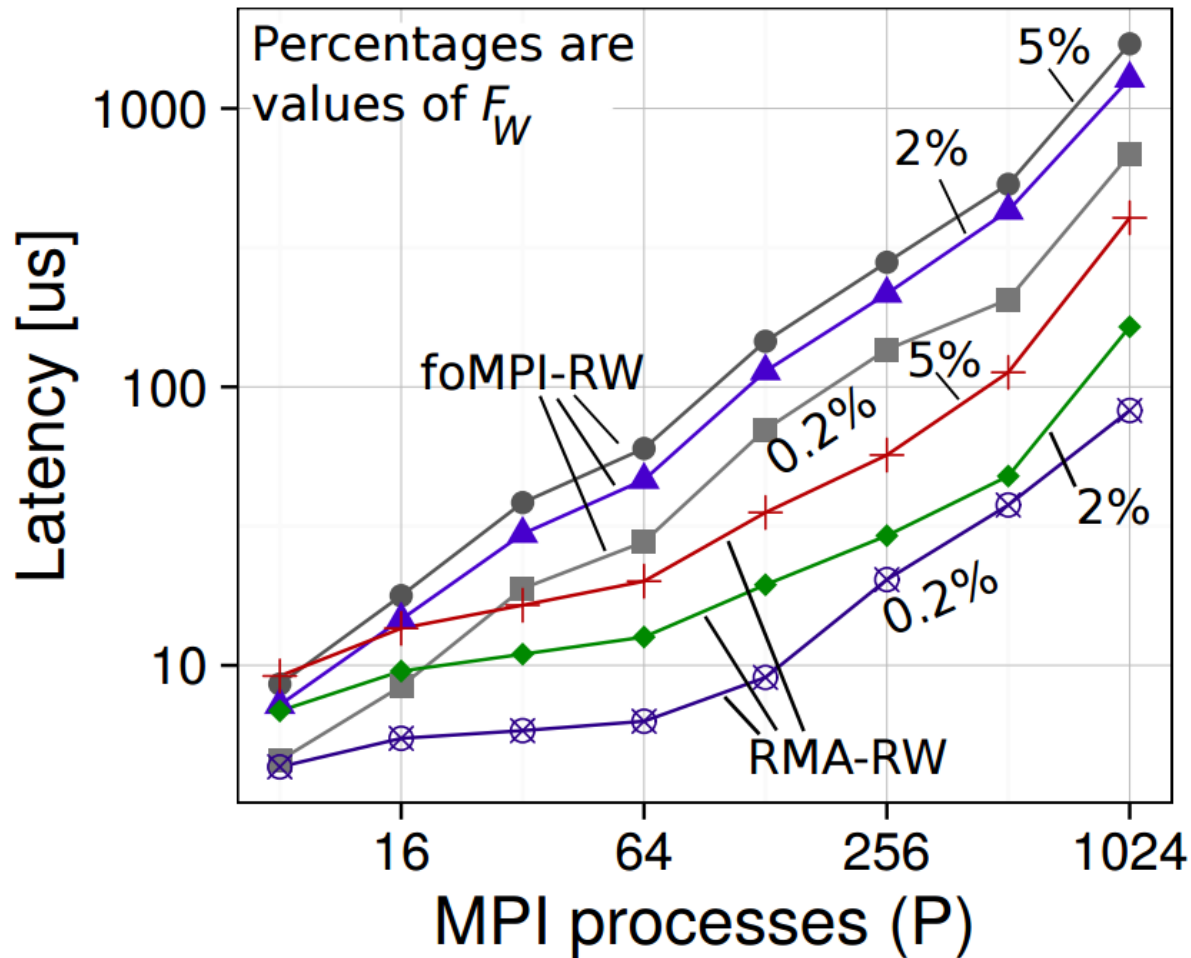
READER THRESHOLD ANALYSIS

Throughput, 0.2% writers,
Empty-critical-section benchmark



EVALUATION

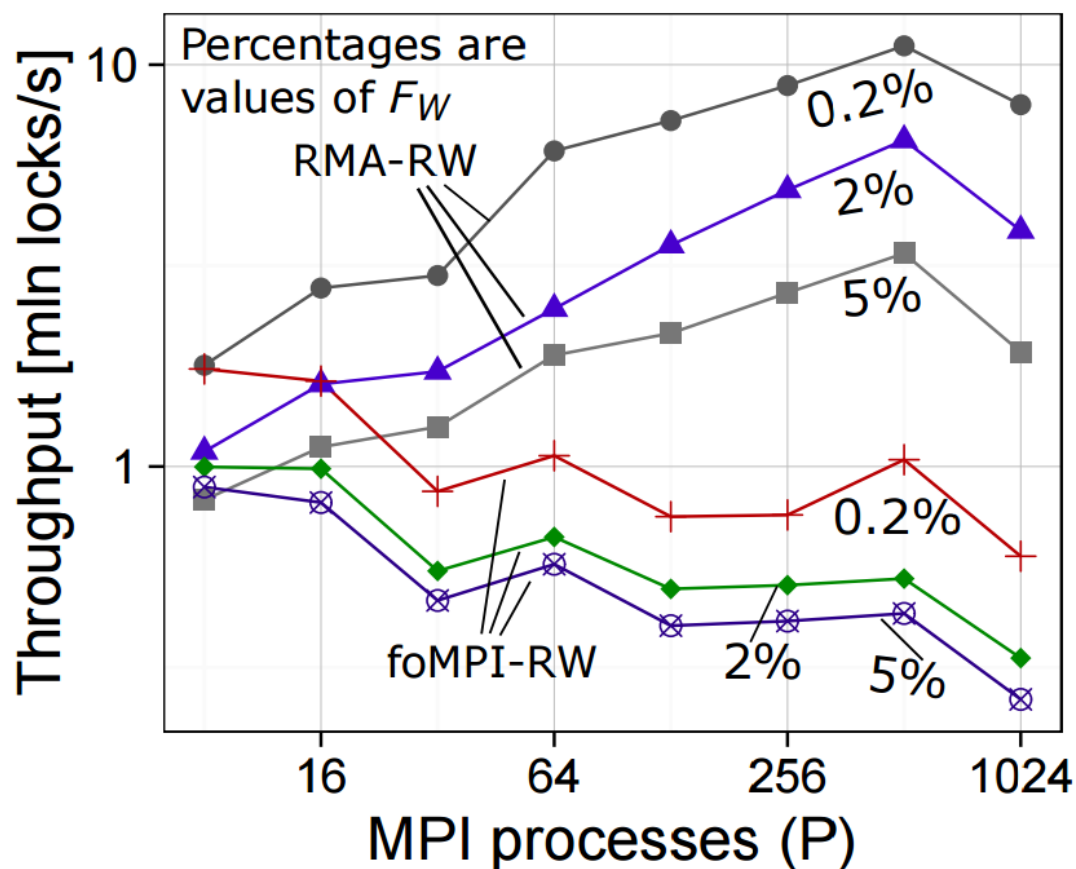
COMPARISON TO THE STATE-OF-THE-ART



EVALUATION

COMPARISON TO THE STATE-OF-THE-ART

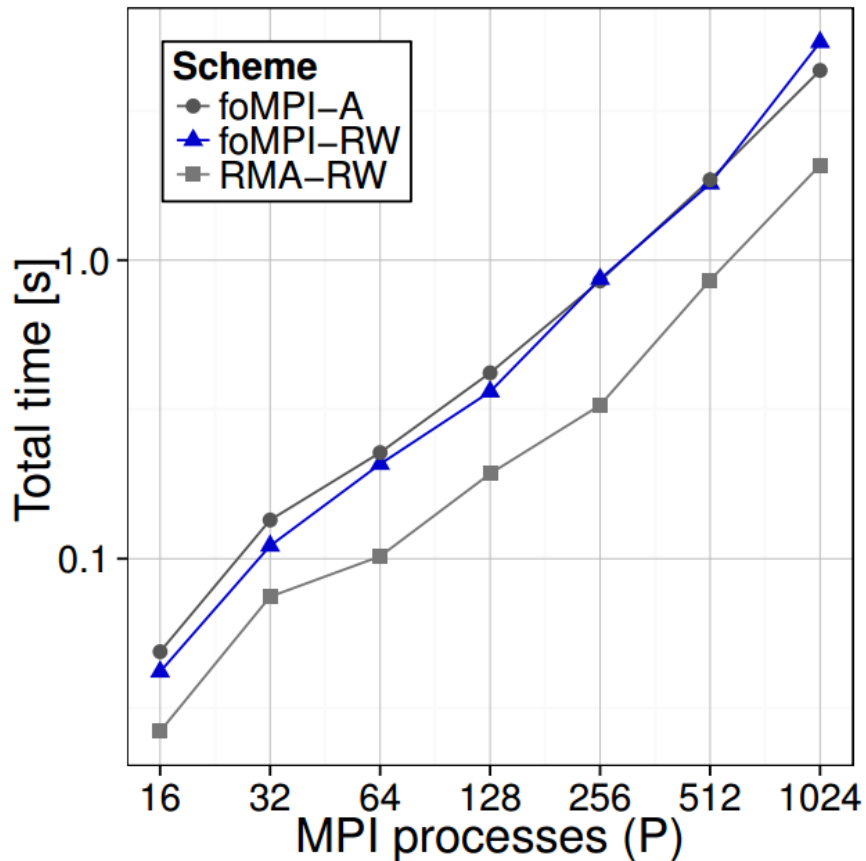
Throughput, single-operation benchmark



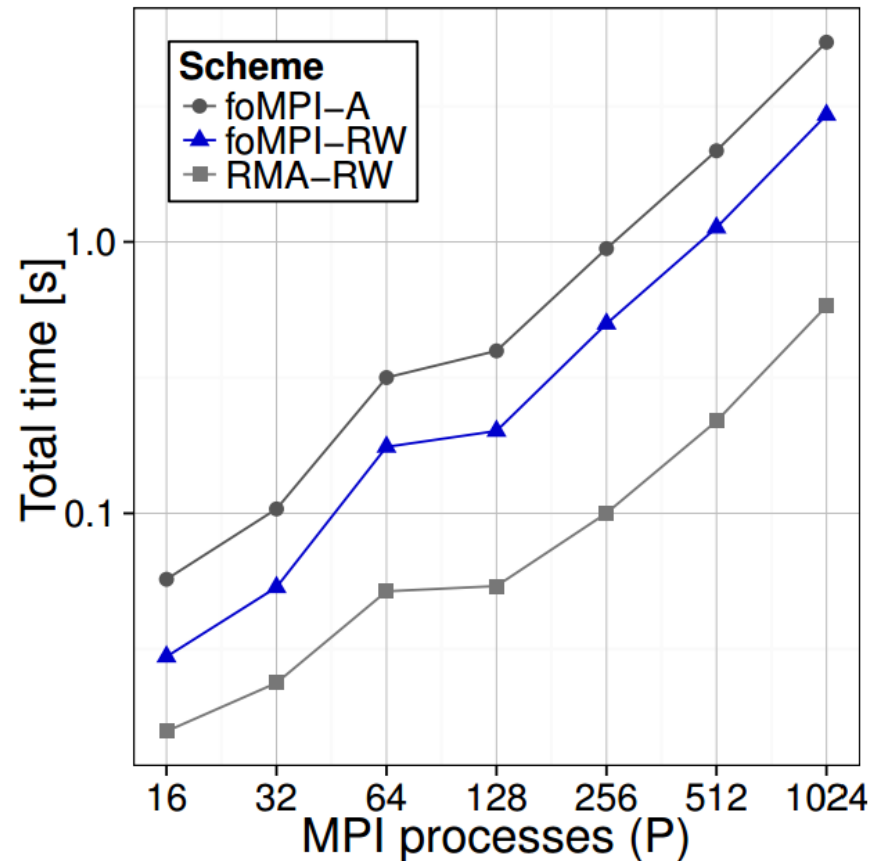
EVALUATION

DISTRIBUTED HASHTABLE

20% writers



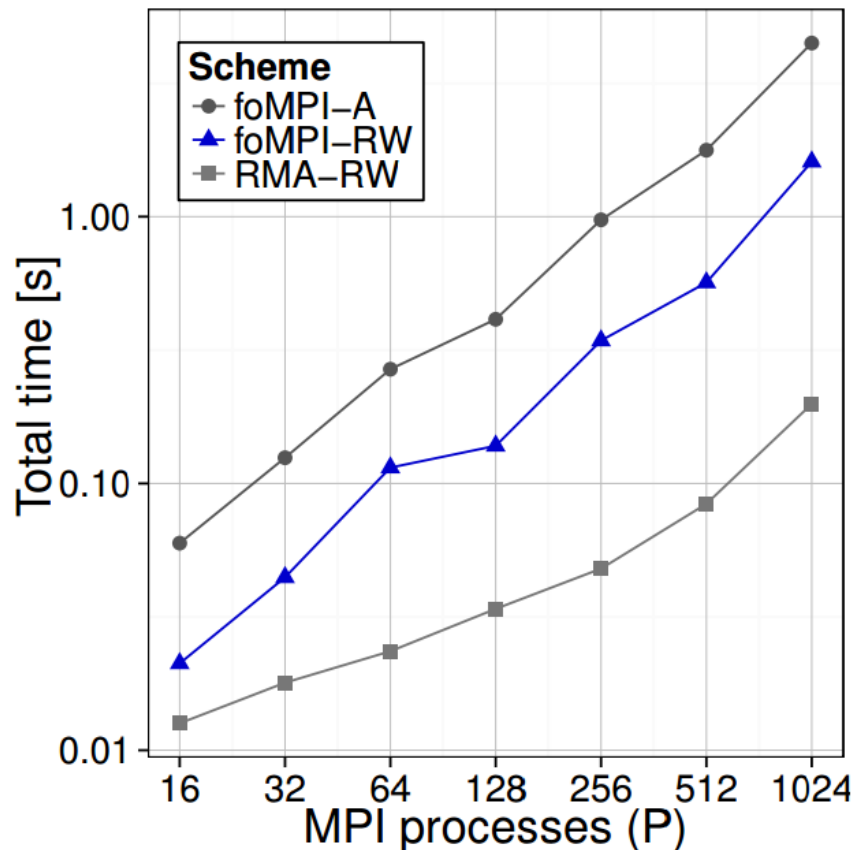
10% writers



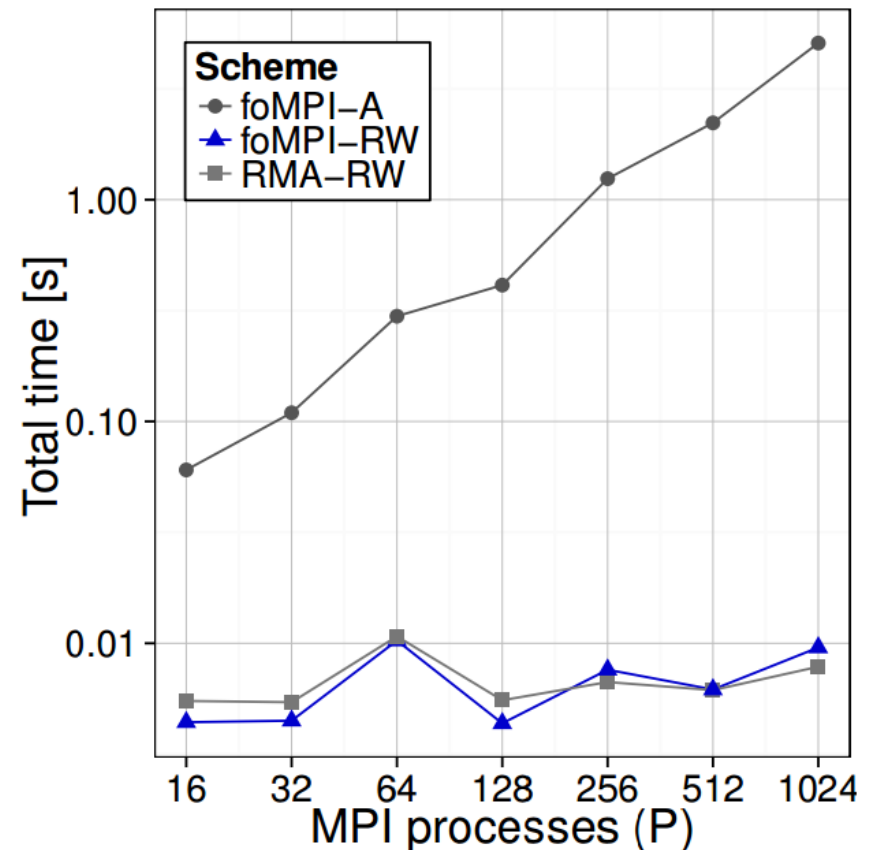
EVALUATION

DISTRIBUTED HASHTABLE

2% of writers



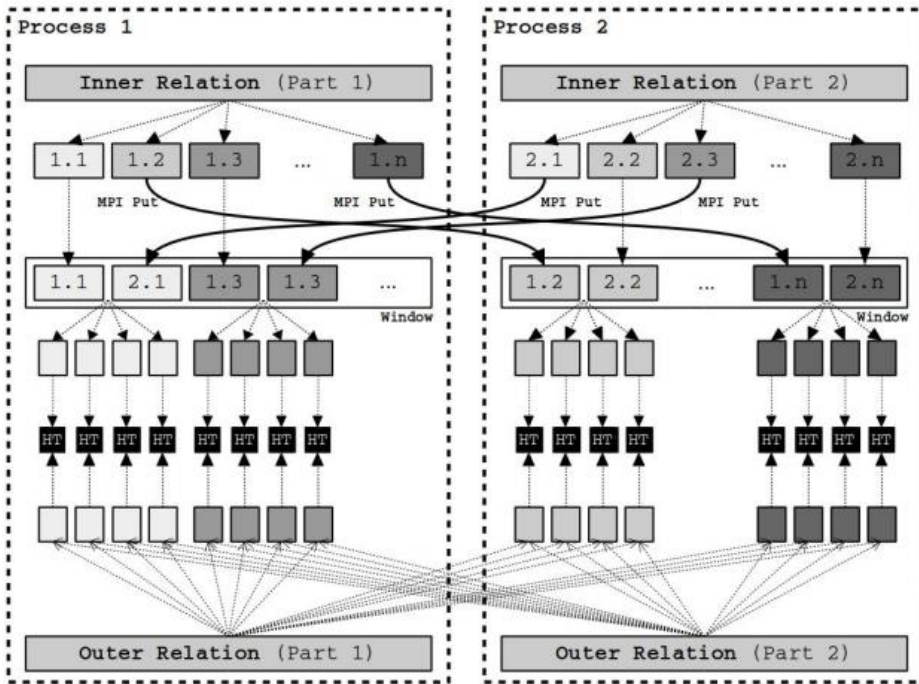
0% of writers



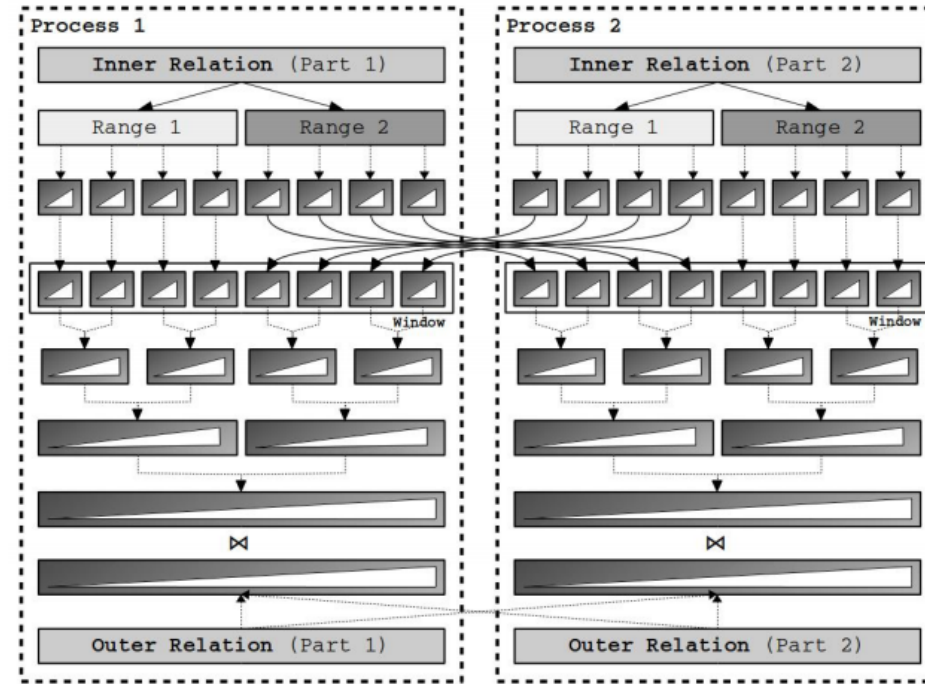
Another application area - Databases

- MPI-RMA for distributed databases?

Hash-Join

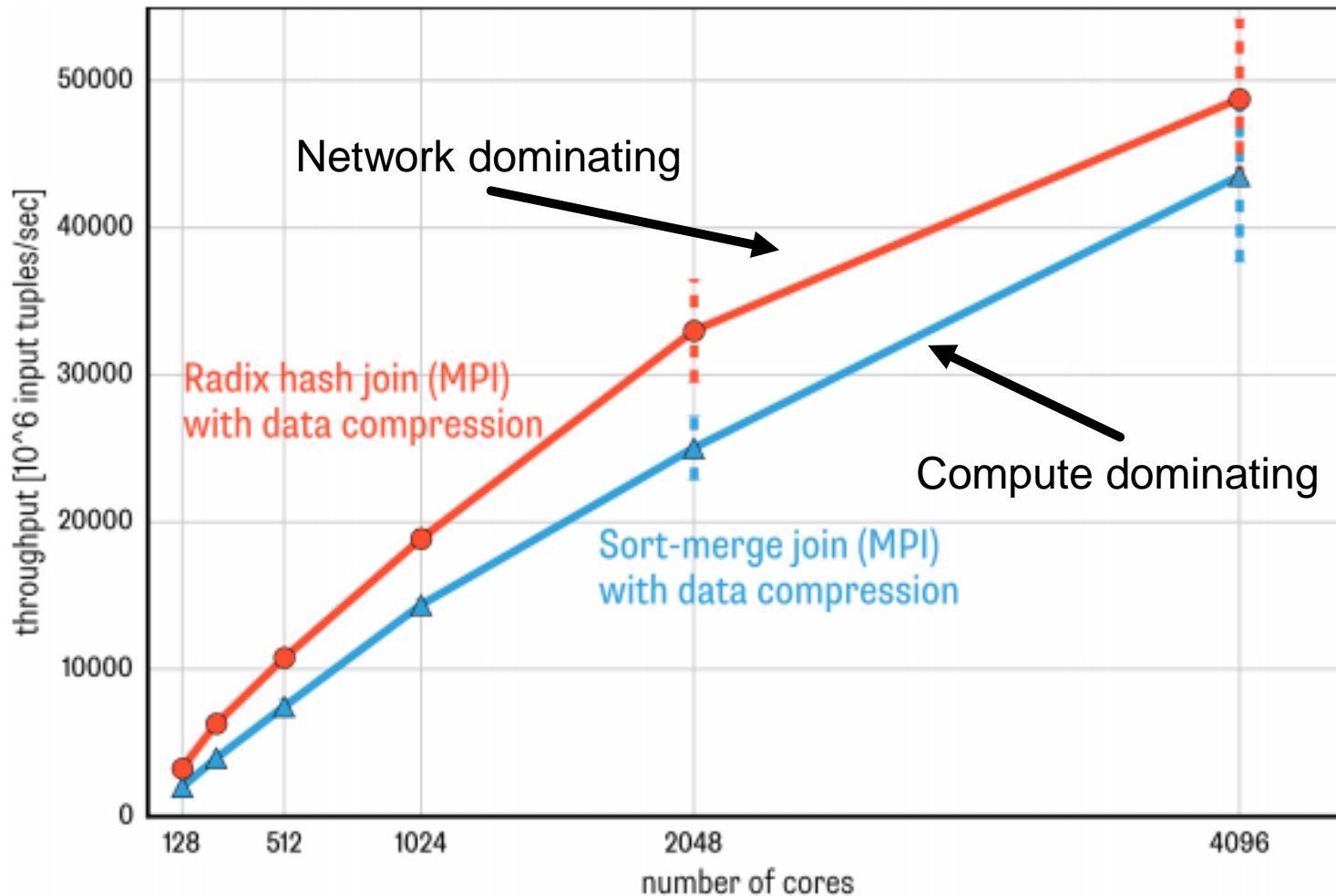


Sort-Join



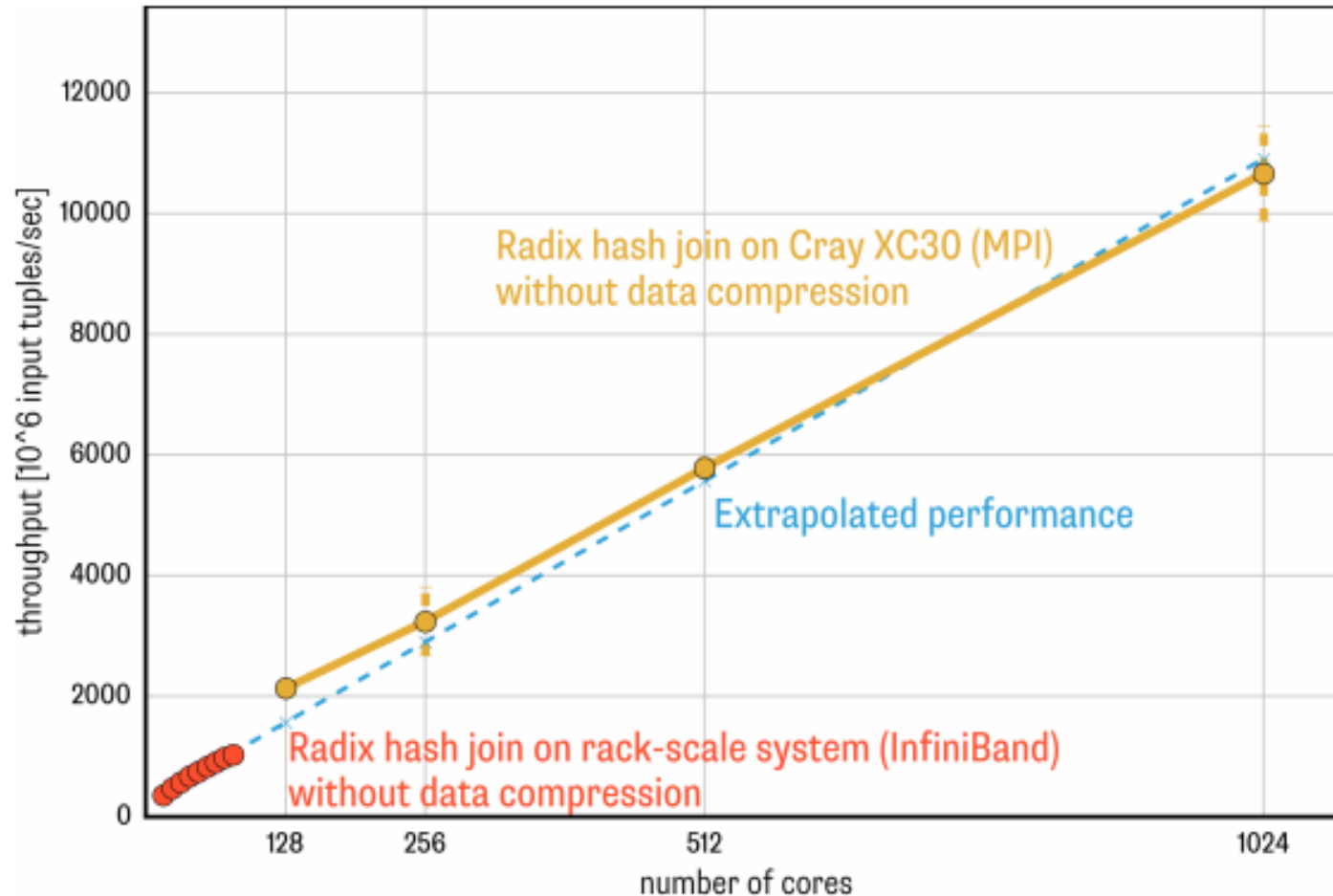
Another application area - Databases

- MPI-RMA for distributed databases on Piz Daint

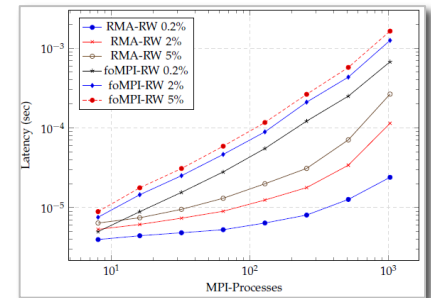
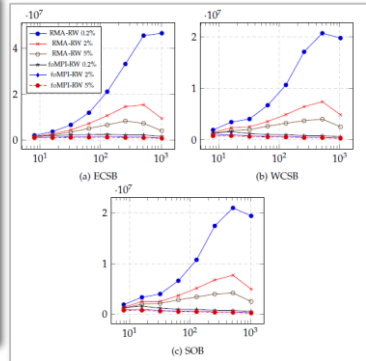
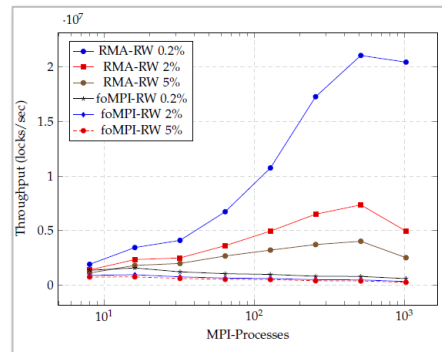
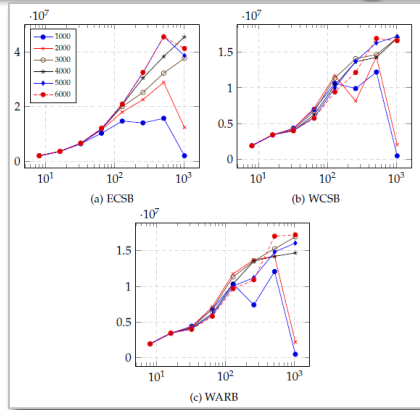
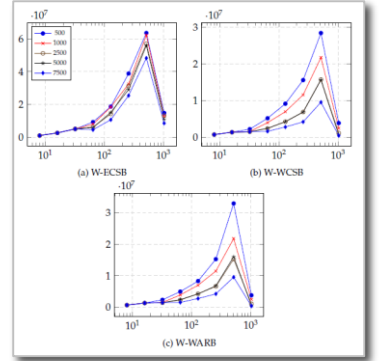
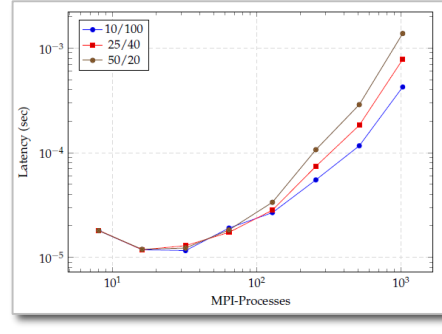
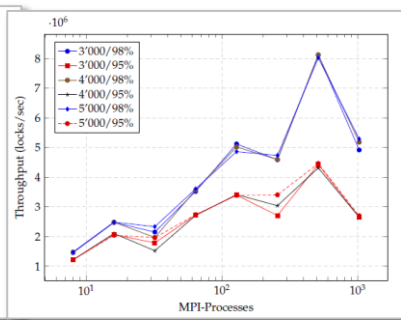
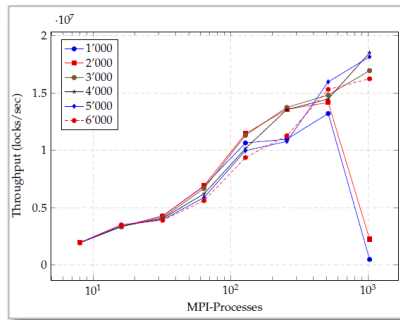
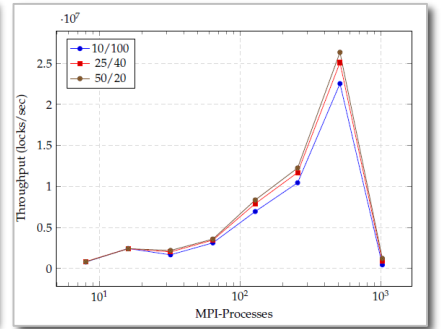
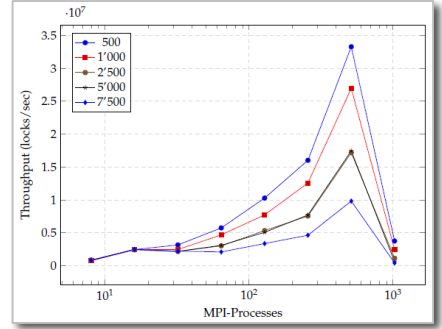
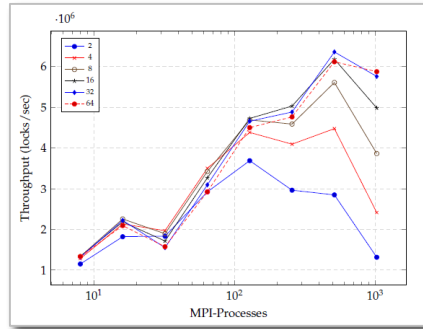
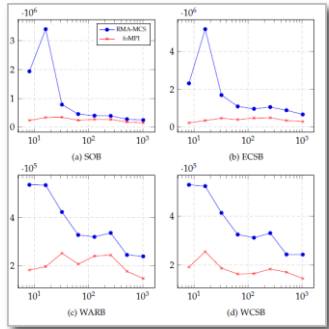


Another application area - Databases

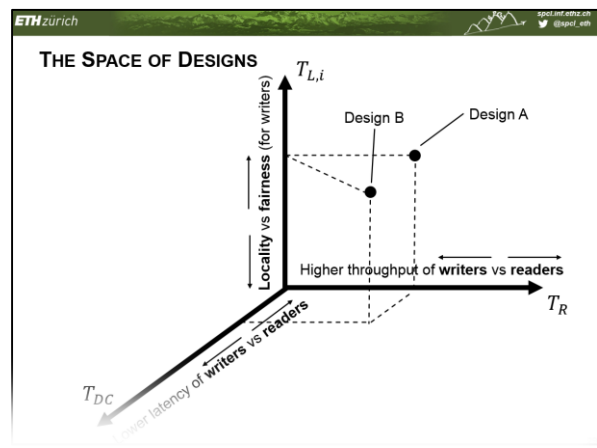
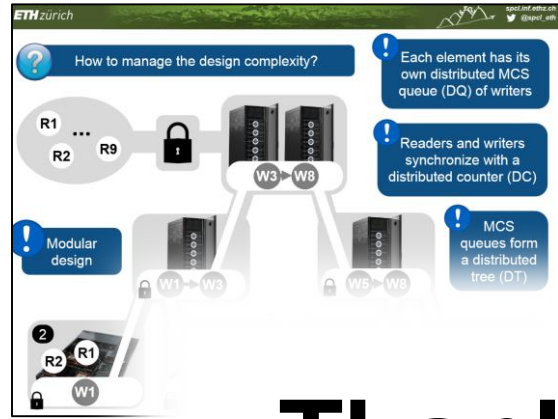
- MPI-RMA for distributed databases on Piz Daint



OTHER ANALYSES



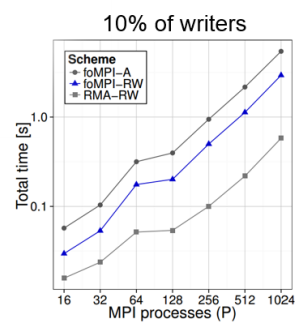
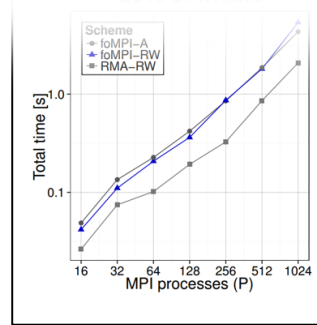
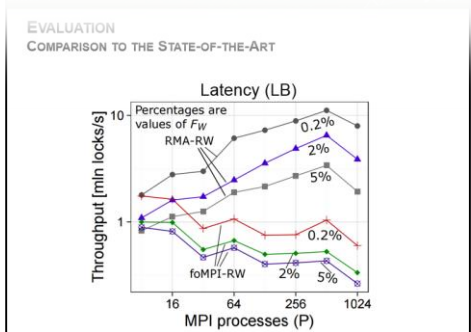
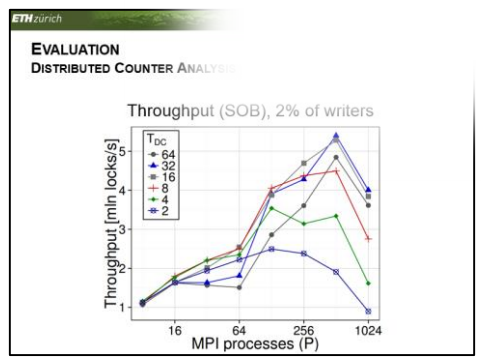
CONCLUSIONS



Thank you for your attention

Modular design
correct

able
ges



Improves latency and throughput over state-of-the-art

Accelerates distributed hashtable