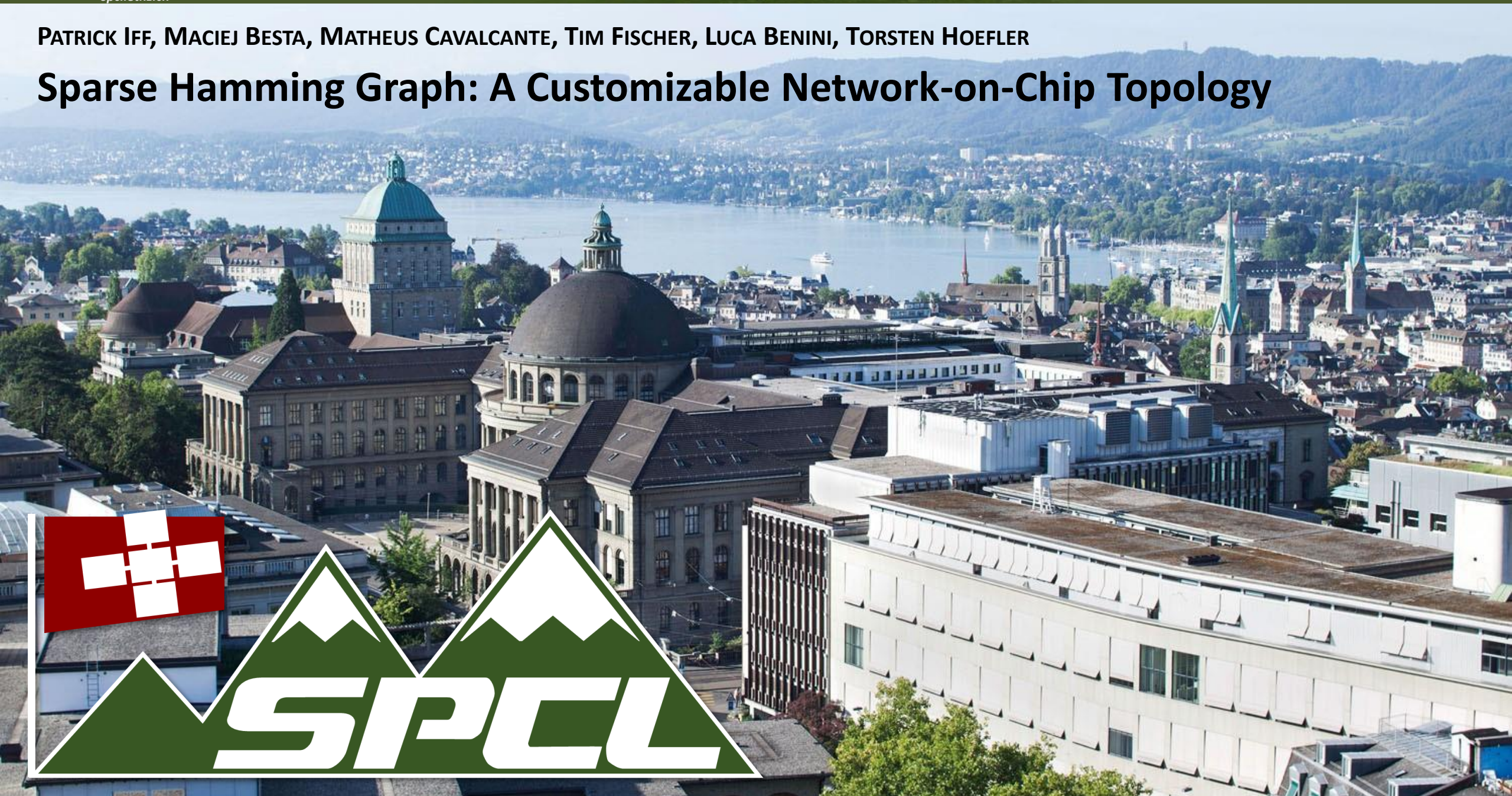
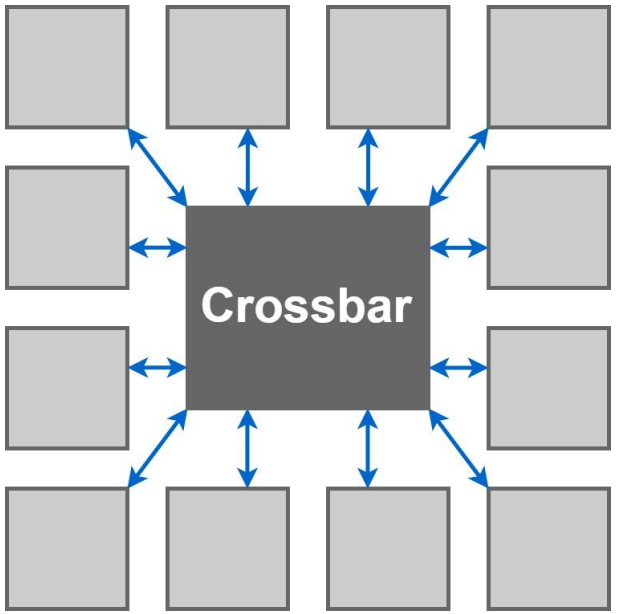
PATRICK IFF, MACIEJ BESTA, MATHEUS CAVALCANTE, TIM FISCHER, LUCA BENINI, TORSTEN HOEFLER

Sparse Hamming Graph: A Customizable Network-on-Chip Topology

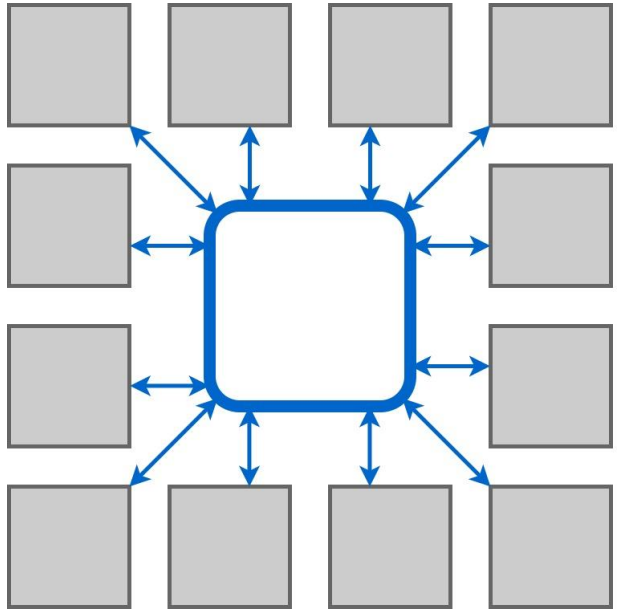


Why Network-on-Chip (NoC)?

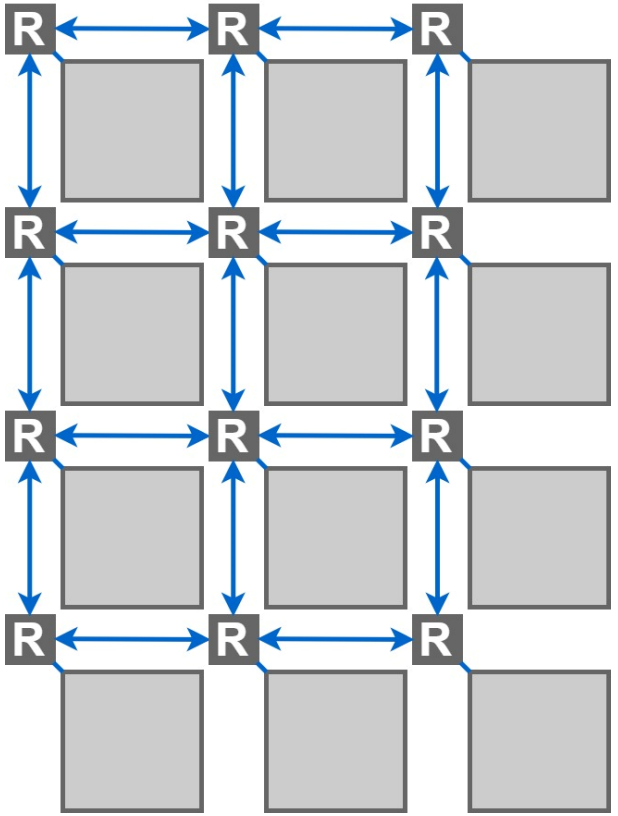
Single Crossbar



Shared Bus

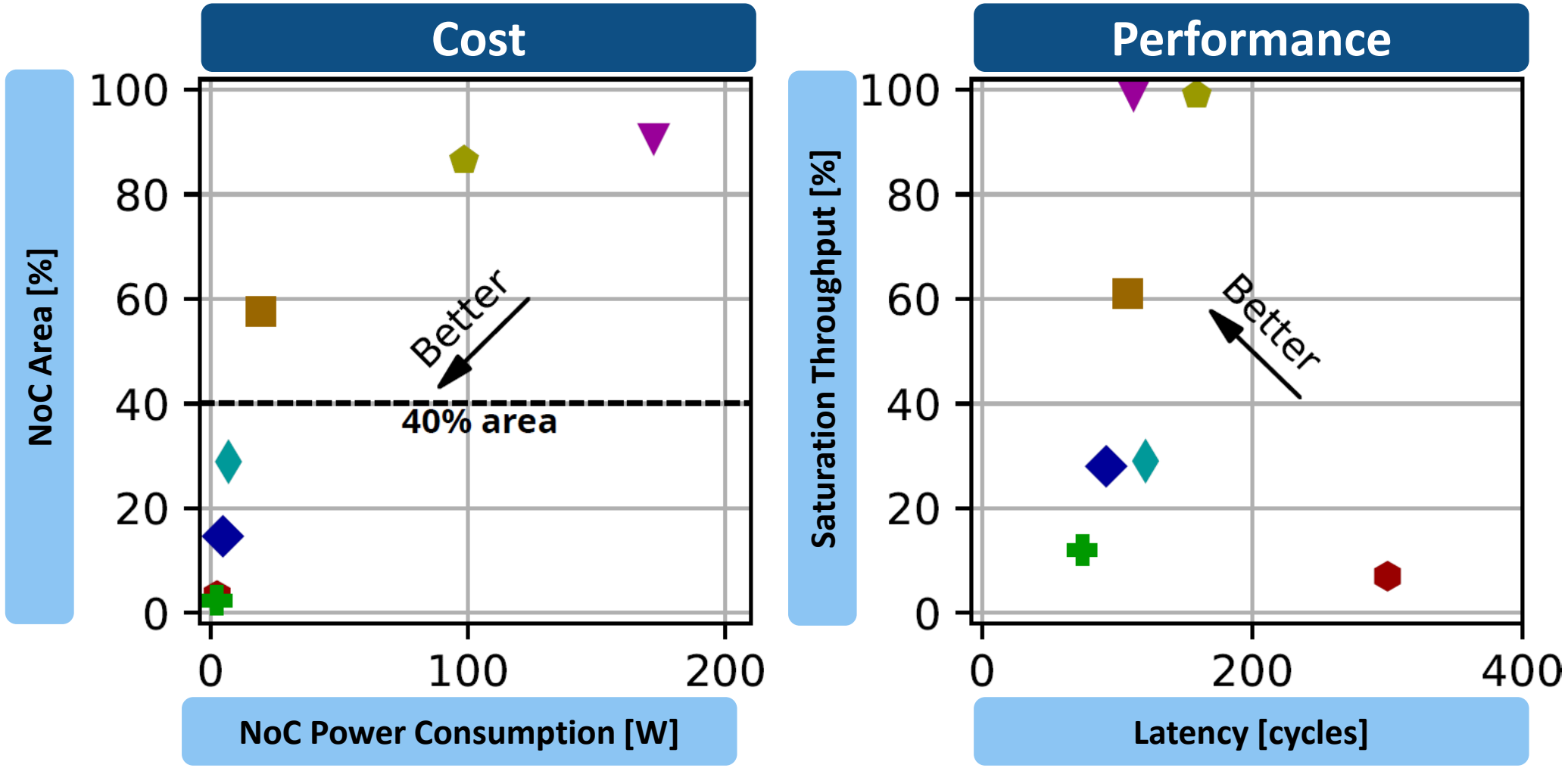


Network-on-Chip (NoC)



Metrics of Interest

Architectural Parameters: 128 tiles (8x16) with 1 core and 35MGE each, 512-bit AXI links, 22nm, uniform traffic, shortest path routing.



Challenge

The NoC topology should be adjusted to the **design goals**

How Architectural Parameters Influence our Metrics of Interest

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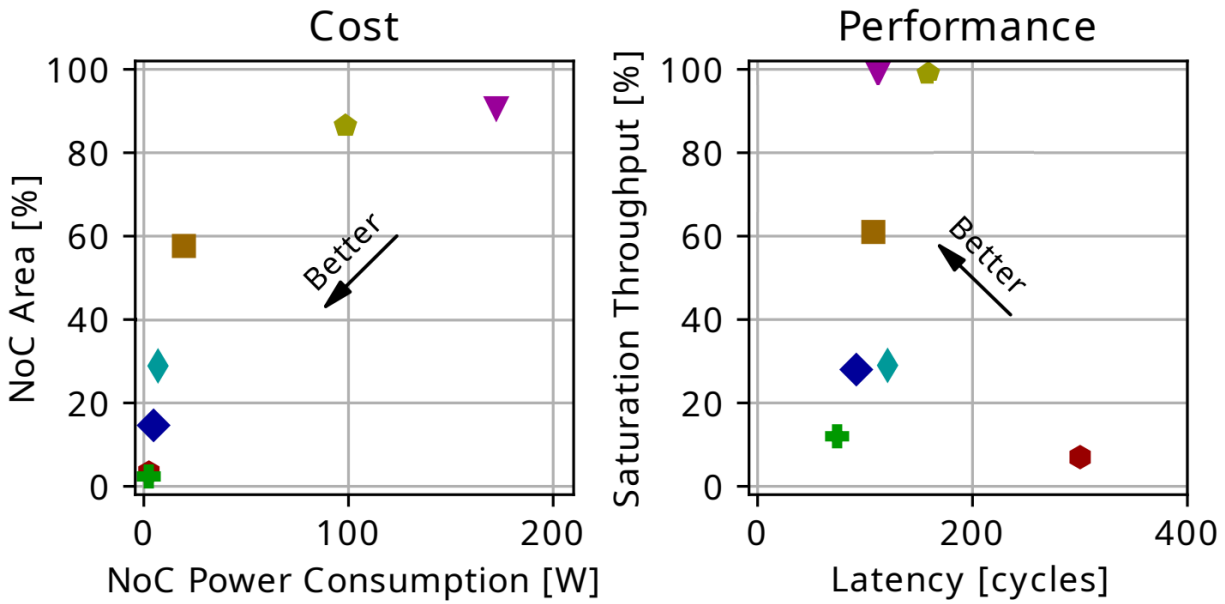
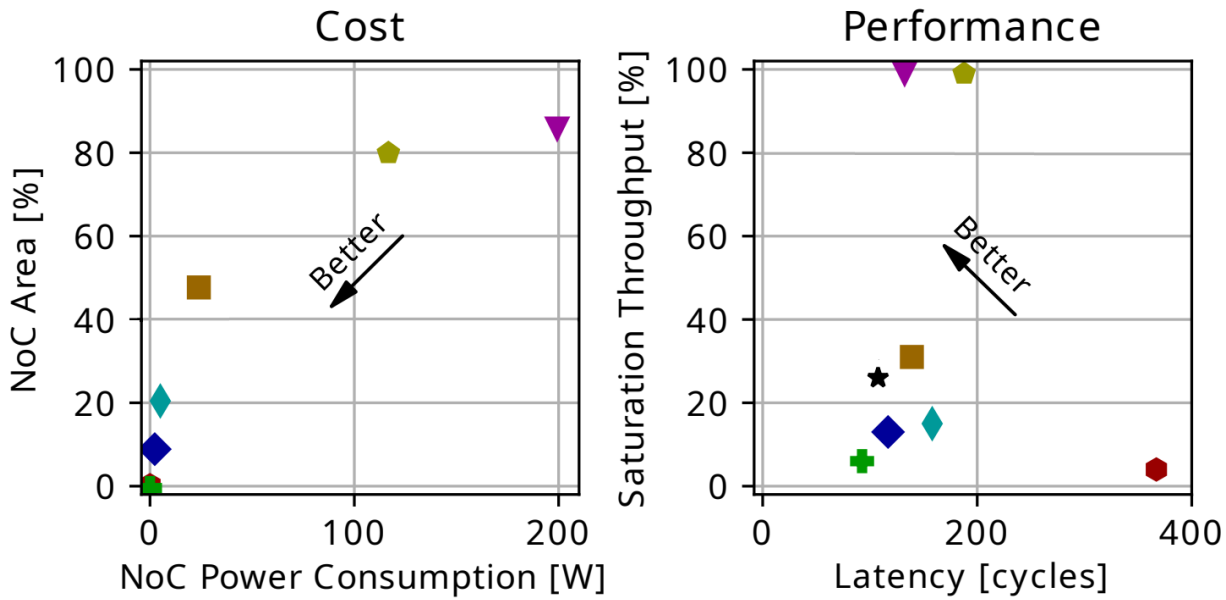


Architectural Parameters : 128 tiles (8x16) with 2 cores and 70MGE each, 512-bit AXI links, 22nm, uniform traffic, shortest path routing.



Ring 2D Mesh 2D Torus Folded 2D Torus Hypercube SlimNoC Flattened Butterfly

Challenges

The NoC topology should be adjusted to the **design goals**

The NoC topology should be adjusted to the **architectural parameters**

Our Contributions

Design Principles for NoC Topologies

The Customizable Sparse Hamming Graph NoC Topology

A fast Toolchain for Cost- and Performance Predictions

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NoC Topology Design Principles

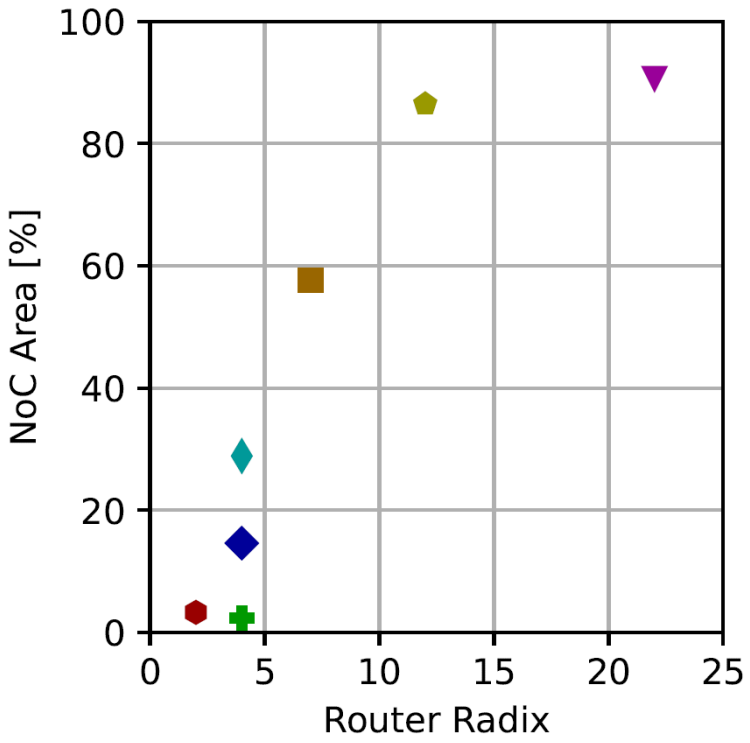
Architectural Parameters: 128 tiles (8x16) with 1 core and 35MGE each, 512-bit AXI links, 22nm, uniform traffic, shortest path routing.

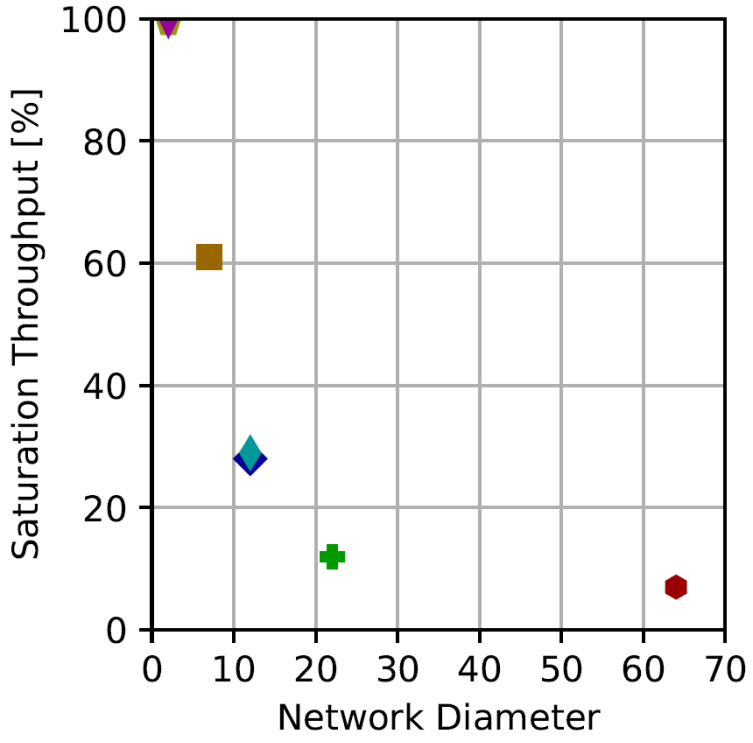
Minimize Cost

1. **Use Low-Radix Topologies**
2. **Design for Routability**

Maximize Performance

3. **Use Low-Diameter Topologies**
4. **Minimize the Physical Path Length**





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SPARSE HAMMING GRAPH: CONSTRUCTION

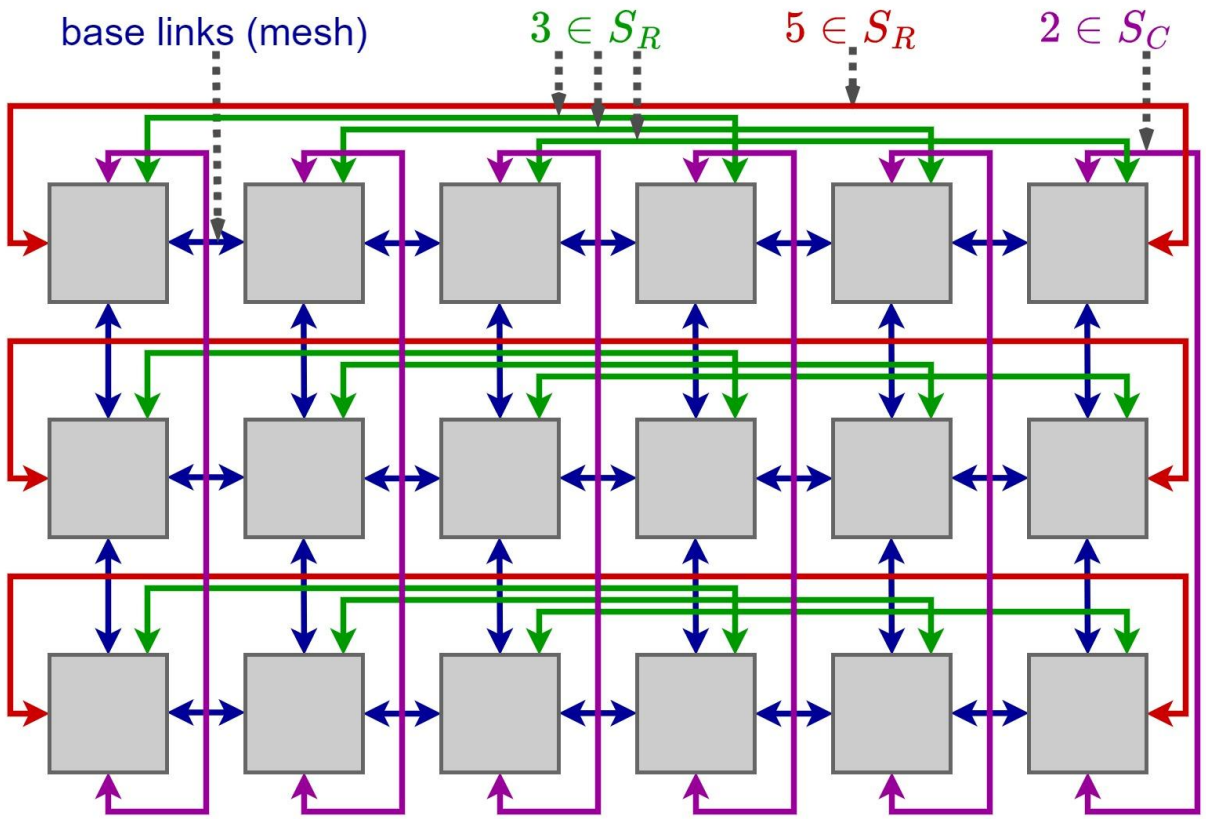
1. Use Low-Radix Topologies
2. Design for Routability
3. Use Low-Diameter Topologies
4. Minimize the Physical Path Length

Specify per-row connectivity:

Set $S_R = \{3, 5\}$

Specify per-column connectivity:

Set $S_C = \{2\}$



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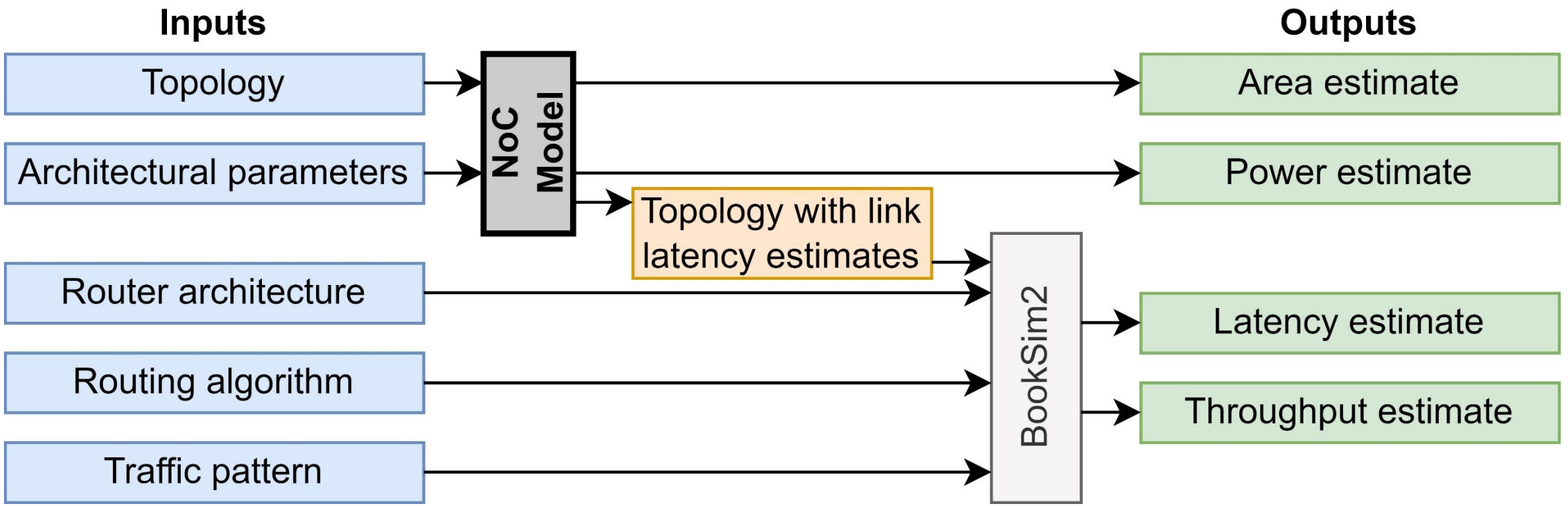
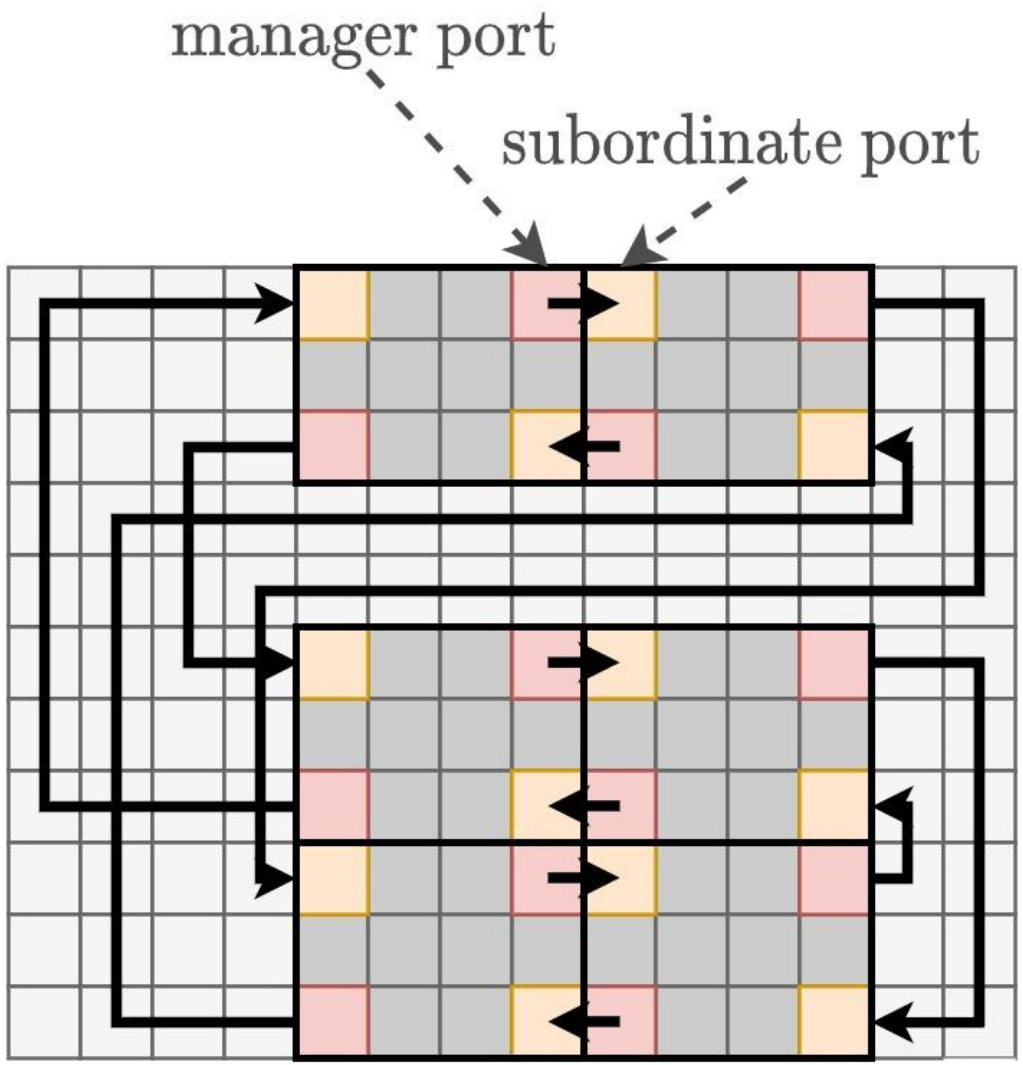
Cost and Performance Prediction Toolchain



Cost and Performance Prediction Toolchain



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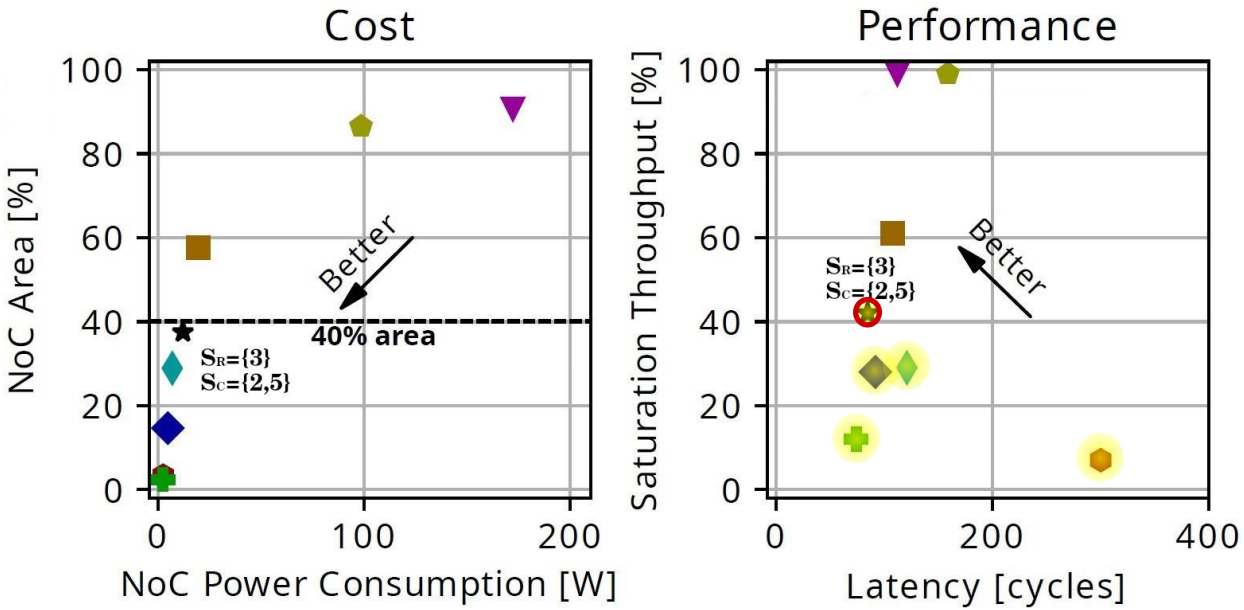
Evaluation

Design Goal Maximize throughput and minimize latency without exceeding a NoC area of 40%

Architectural Parameters: 128 tiles (8x16) with 1 core and 35MGE each, 512-bit AXI links, 22nm, uniform traffic, shortest path routing.



Ring 2D Mesh 2D Torus Folded 2D Torus Hypercube SlimNoC Flattened Butterfly Sparse Hamming Graph (This Work)

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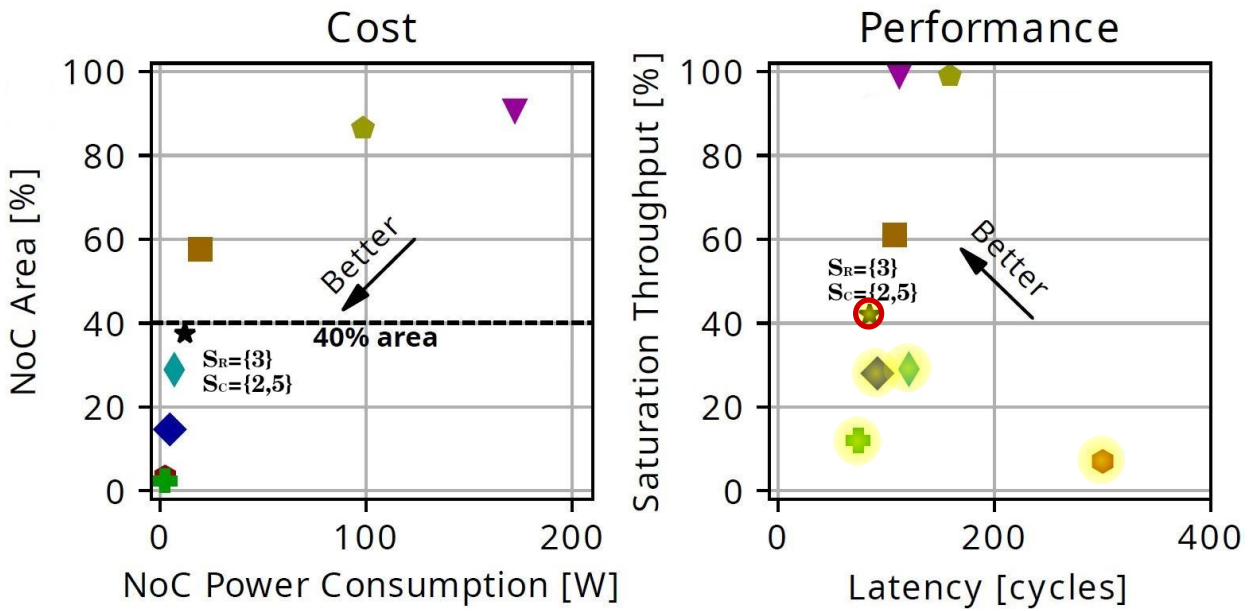

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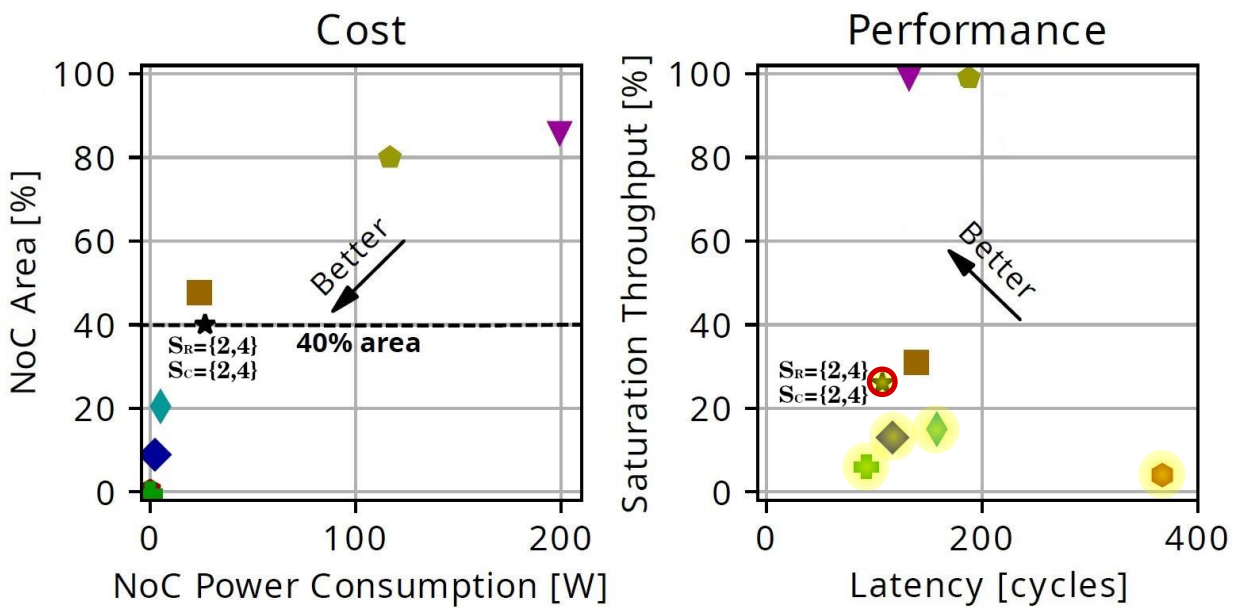

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Conclusions

We facilitate adjusting the NoC topology to design goals and architectural parameters by providing…

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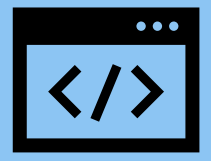

A fast Toolchain for Cost- and Performance Predictions

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